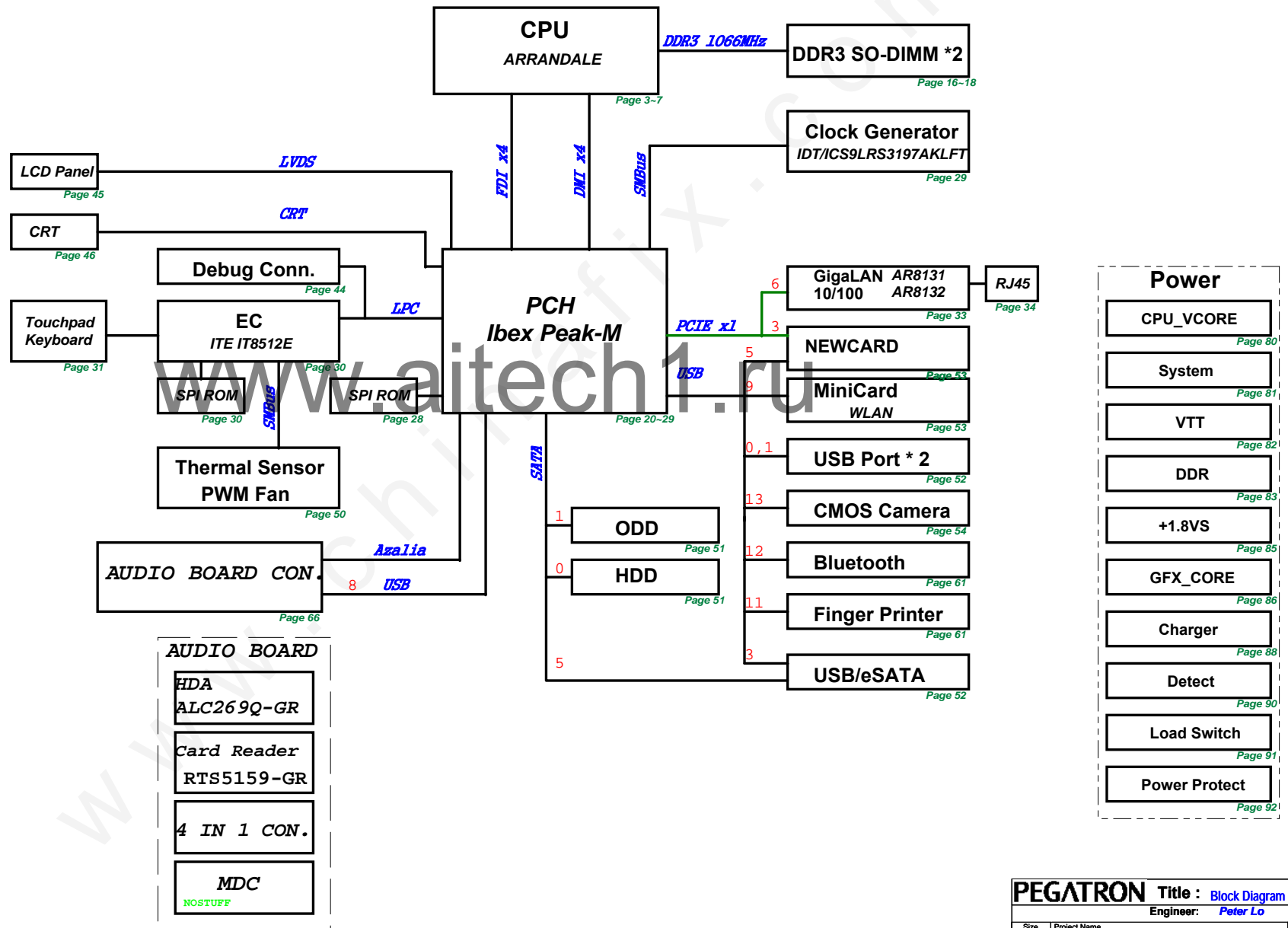


H24Y Capella Platform w/o iAMT Rev. 1.0 BLOCK DIAGRAM



PCH_IBEX GPIO						EC IT8512			EC IT8301		
PCH_IBEX GPIO	Use As	Signal Name	Internal & External Pull-up/down	Power		EC GPIO	Use As	Signal Name	EC GPIO	Use As	Signal Name
GPIO 00	-	-	-	+3VS		GPA0		PWR_LED#	GPIO0	-	-
GPIO 01	-	-	INT TBD	+3VS		GPA1		CHG_LED#	GPIO1	-	-
GPIO [2:5]	-	-	EXT PU	+5VS		GPA2	-	-	GPIO2	-	-
GPIO 06	-	-	INT TBD	+3VS		GPA3	-	-	GPIO3	-	-
GPIO 07	-	-	INT TBD	+3VS		GPA4	LCD_BL_PWM		GPIO4	ME_+VM_PWRGD	
GPIO 08	GPI	EXT_SMI#	EXT PU & INT PU	+3VSUS		GPA5	FAN0_PWM		GPIO5	ME_PM_SLP_LAN#	
GPIO 09	-	-	EXT PU	+3VSUS		GPA6	BAT1_CNT1#		GPIO6	ME_AC_PRESENT	
GPIO 10	-	-	EXT PU	+3VSUS		GPA7	BAT2_CNT1#		GPIO7	-	-
GPIO 11	GPI	EXT_SCI#	EXT PU	+3VSUS		GPB0	SUSC_EC#		GPIO8	-	-
GPIO 12	Native	LAN_PHY_PWR_CTRL	EXT PU	+3VSUS		GPB1	SUSB_EC#		GPIO9	-	-
GPIO 13	-	-	-	+3VSUS		GPB2	CTX0		GPIO10	-	-
GPIO 14	-	-	EXT PU	+3VSUS		GPB3	SMB0_CLK		GPIO11	ME_LAN_RST#	
GPIO 15	GPO	WLAN_ON	INT PD	+3VSUS		GPB4	SMB0_DAT		GPIO12	ME_PWROK	
GPIO 16	-	-	-	+3VS		GPB5	A20GATE		GPIO13	ME_WLAN_PWR_ON	
GPIO 17	GPO	WLAN_LED	EXT PD & INT TBD	+3VS		GPB6	RC_IN#		GPIO14	ME_SLP_M_EC#	
GPIO 18	Native	PCIECLKRQ1#	EXT PU	+3VS		GPB7	PM_RSMRST#		GPIO15	-	-
GPIO 19	-	-	-	+3VS		GPC0	CRX0		GPIO16	-	-
GPIO 20	Native	PCIECLKRQ2#	EXT PU	+3VS		GPC1	SMB1_CLK		GPIO17	-	-
GPIO 21	-	-	-	+3VS		GPC2	SMB1_DAT		GPIO18	-	-
GPIO 22	GPI	BT_DET#	EXT PU	+3VS		GPC3	PM_PWRBTN#		GPIO19	-	-
GPIO 23	-	-	INT PU	+3VS		GPC4	AC_IN_OC#		GPIO20	-	-
GPIO 24	-	-	-	+3VSUS		GPC5	OP_SD#		GPIO21	-	-
GPIO 25	Native	PCIECLKRQ3#	EXT PU	+3VSUS		GPC6	BAT1_IN_OC#		GPIO22	-	-
GPIO 26	-	-	EXT PU (Not used)	+3VSUS		GPC7	RFON_SW#		GPIO23	-	-
GPIO 27	GPO	BT_ON	INT WEAK PU	+3VSUS		GPD0	PWRLIMIT#		GPIO24	-	-
GPIO 28	GPO	BT_LED	EXT PD	+3VSUS		GPD1	PM_SUSC#		GPIO25	-	-
GPIO 29	Native	SLP_LAN#	-	+3VSUS		GPD2	BUF_PLT_RST#		GPIO26	-	-
GPIO 30	Native	SUS_PWR_ACK	-	+3VSUS		GPD3	EXT_SCI#		GPIO27	-	-
GPIO 31	Native	ACPRESENT	-	+3VSUS		GPD4	EXT_SMI#		GPIO28	-	-
GPIO 32	Native	CLKRUN#	-	+3VS		GPD5	LCD_BACKOFF#		GPIO29	-	-
GPIO 33	-	-	-	+3VS		GPD6	FAN0_TACH		GPIO30	-	-
GPIO 34	Native	STP_PCI#	-	+3VS		GPD7	COLOREN#		GPIO31	-	-
GPIO 35	-	-	-	+3VS		GPE0	VSUS_ON		GPIO32	-	-
GPIO 36	-	-	-	+3VS		GPE1	EGAD (IT8301 Address/Data connect)		GPIO33	-	-
GPIO 37	GPI	PCB_ID0/SPIROM_ID0	EXT PD	+3VS		GPE2	EGCS (IT8301 Cycle Start connect)		GPIO34	-	-
GPIO 38	GPI	PCB_ID1/SPIROM_ID1	EXT PD	+3VS		GPE3	EGCLK (IT8301 Clock connect)		GPIO35	-	-
GPIO 39	GPI	PCB_ID2	EXT PD	+3VS		GPE4	PWR_SW#		GPIO36	-	-
GPIO 40	-	-	EXT PU (Not used)	+3VSUS		GPE5	BAT2_IN_OC#		GPIO37	-	-
GPIO 41	-	-	EXT PU (Not used)	+3VSUS		GPE6	LID_SW#				
GPIO 42	-	-	EXT PU (Not used)	+3VSUS		GPE7	CAP_ACK#				
GPIO 43	-	-	EXT PU (Not used)	+3VSUS		GPFO	Instant Button1/BLUETOOTH#/EMAIL#				
GPIO 44	-	-	EXT PU (Not used)	+3VSUS		GPF1	Instant Button2/INTERNET#/WLAN#				
GPIO 45	-	-	EXT PU (Not used)	+3VSUS		GPF2	IInstant Button3/ MARATHON#				
GPIO 46	-	-	EXT PU (Not used)	+3VSUS		GPF3	Instant Button4/ DISTP#				
GPIO 47	Native	PEG_A_CLKRQ#	EXT PD	+3VSUS		GPF4	TP_CLK				
GPIO 48	-	-	-	+3VS		GPF5	TP_DAT				
GPIO 49	-	-	-	+3VS		GPF6	THRO_CPU				
GPIO 50	-	-	EXT PU (Not used)	+5VS		GPF7	-				
GPIO 51	-	-	INT PU	+3VS		GG0	PM_THERM#				
GPIO 52	-	-	-	+5VS		GPG1	PM_SUSB#				
GPIO 53	-	-	INT PU	+3VS		GPG2	BAT1_CNT2#				
GPIO 54	-	-	-	+5VS		GPG6	BAT2_CNT2#				
GPIO 55	-	-	INT PU	+3VS		GPH0	PM_CLKRUN#				
GPIO 56	Native	PEG_B_CLKRQ#	EXT PU	+3VSUS		GPH1	-				
GPIO 57	-	-	-	+3VSUS		GPH2	GFX_VR_ON				
GPIO 58	Native	SML1CLK	-	+3VSUS		GPH3	BAT_LEARN				
GPIO 59	-	-	EXT PU (Not used)	+3VSUS		GPH4	SCRL_LED#				
GPIO 60	-	-	-	+3VSUS		GPH5	NUM_LED#				
GPIO 61	-	-	-	+3VSUS		GPH6	CAP_LED#				
GPIO 62	-	-	-	+3VSUS		GPI0	VGA_ALERT#				
GPIO 63	-	-	-	+3VSUS		GPI1	SUS_PWRGD				
GPIO 64	Native	CLKOUTFLEX0	INT TBD	+3VS		GPI2	ALL_SYSTEM_PWRGD				
GPIO 65	Native	CLKOUTFLEX1	INT TBD	+3VS		GPI3	VRM_PWRGD				
GPIO 66	-	-	INT TBD	+3VS		GPI4	GFX_VR				
GPIO 67	-	-	INT TBD	+3VS		GPI5	ALS_AD				
GPIO 72	-	-	-	+3VSUS		GPI6	KB_ID0				
GPIO 73	-	-	EXT PU (Not used)	+3VSUS		GPI7	KB_ID1				
GPIO 74	-	-	EXT PU (Not used)	+3VSUS		GPJ0	CPU_VRON				
GPIO 75	Native	SML1DATA	-	+3VSUS		GPJ1	PM_PWROK				
						GPJ2	VSET_EC				
						GPJ3	ISET_EC				
						GPJ4	TP_LED				
						GPJ5	FAN_DA				

SM_BUS ADDRESS :

SM-Bus Device	SM-Bus Address
Clock Generator	1101001x (D2h)
SO-DIMM 0	1010000x (A0h)
SO-DIMM 1	1010001x (A4h)
CPU Thermal IC(G780)	1001100x (98h)
VGA Thermal IC(G781-1)	1001101x (9Ah)
VGA Thermal Sensor(NB9E-GE1)	1001111x (9Eh)
VID Controller ASM8272	0011011x (36h)
DSP FM2010	

PCIE 1	Minicard TV Tuner	USB 0	USB Port (1)
PCIE 2	Minicard WLAN	USB 1	USB Port (2)
PCIE 3	Newcard	USB 2	USB Port (3)
PCIE 4	N/A	USB 3	USB Port (4)
PCIE 5	PCIE to SATA (SR)	USB 4	CMOS Camera
PCIE 6	GLAN	USB 5	Newcard
PCIE 7	N/A	USB 6	Minicard TV Tuner
PCIE 8	N/A	USB 7	N/A
		USB 8	OLED
		USB 9	WLAN
		USB 10	N/A
		USB 11	USB Port (5)
		USB 12	Bluetooth
		USB 13	Finger Print

SATA0	SATA HDD(1)
SATA1	SATA ODD
SATA2	N/A
SATA3	N/A
SATA4	SATA HDD(2)
SATA5	eSATA

Size	Project Name	Rev
Custom	H24Y	1.0

PEGATRON

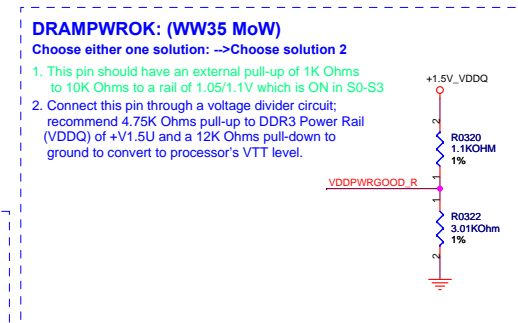
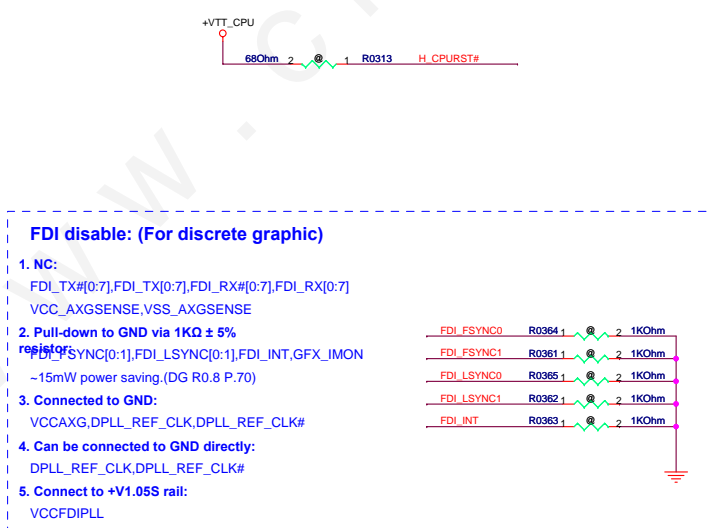
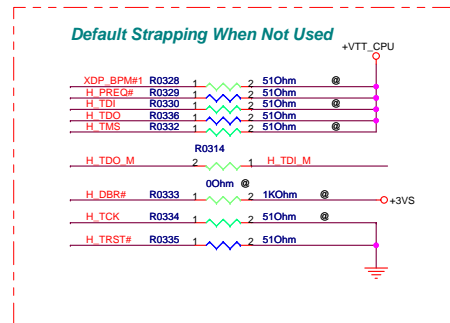
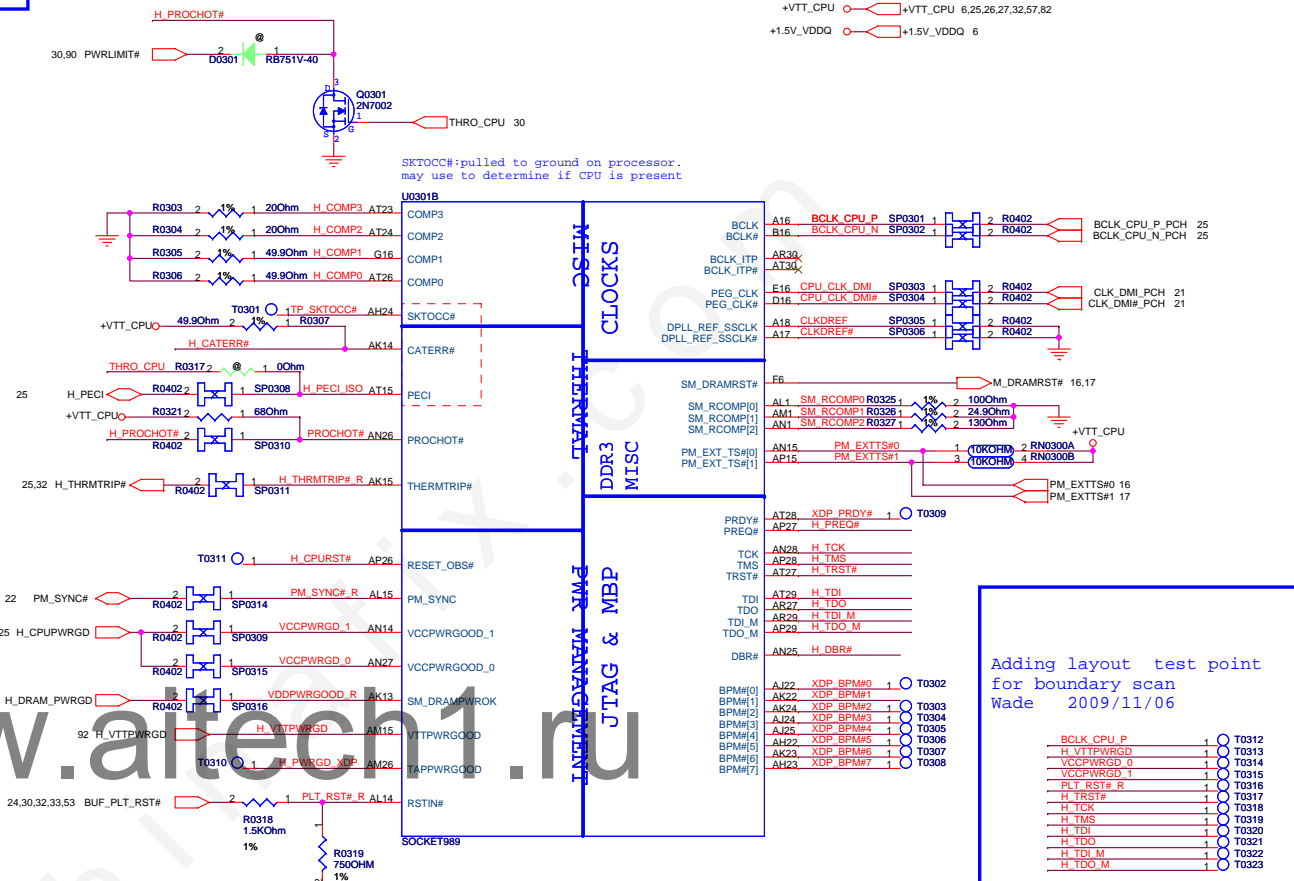
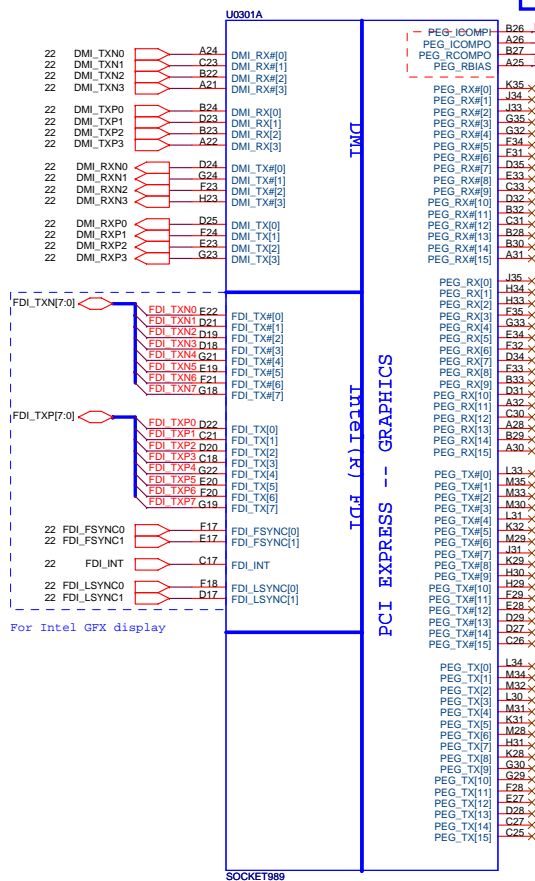
Title : System Setting

Engineer: Peter Lo

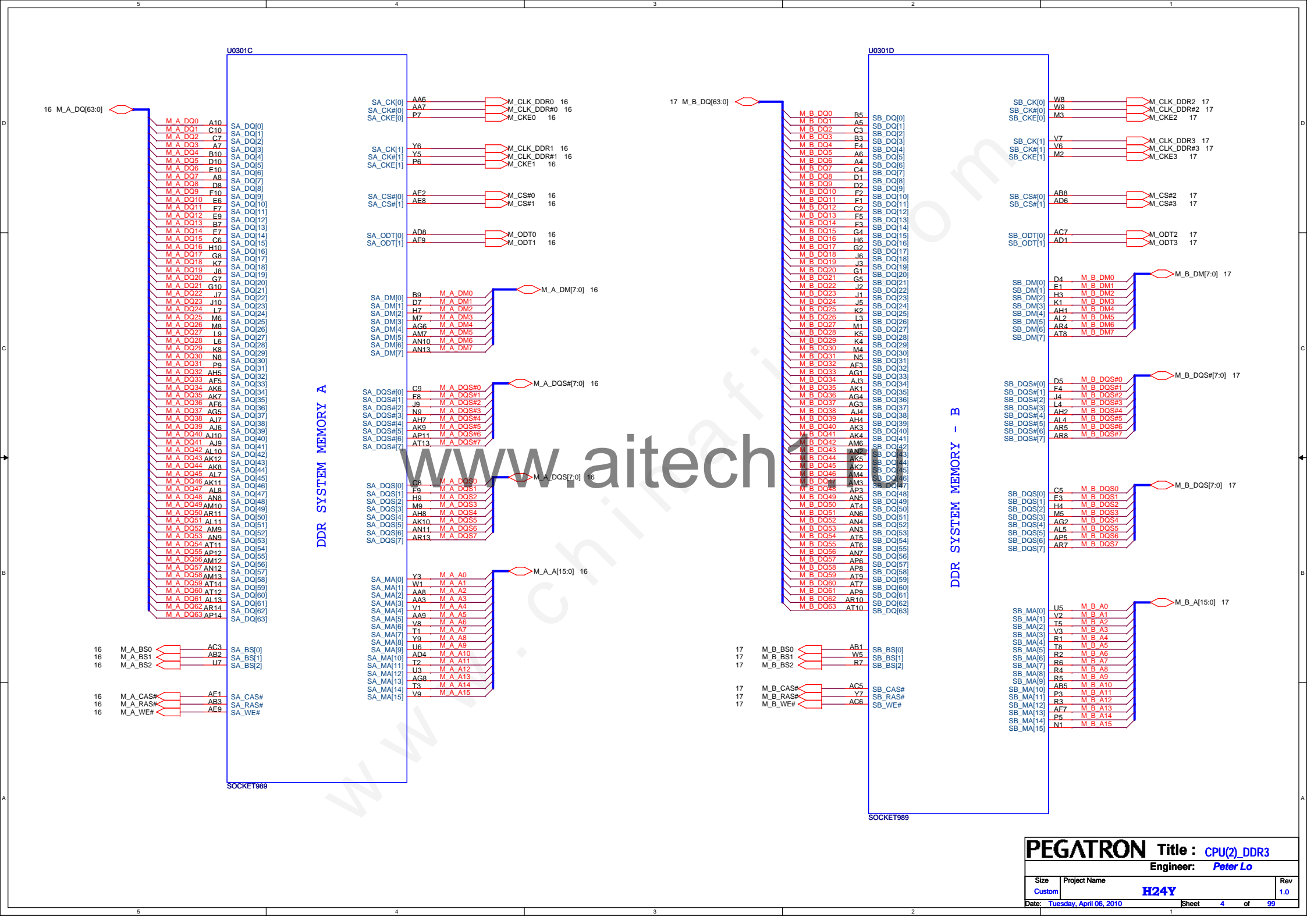
Date: Friday, March 12, 2010

Sheet 2 of 99

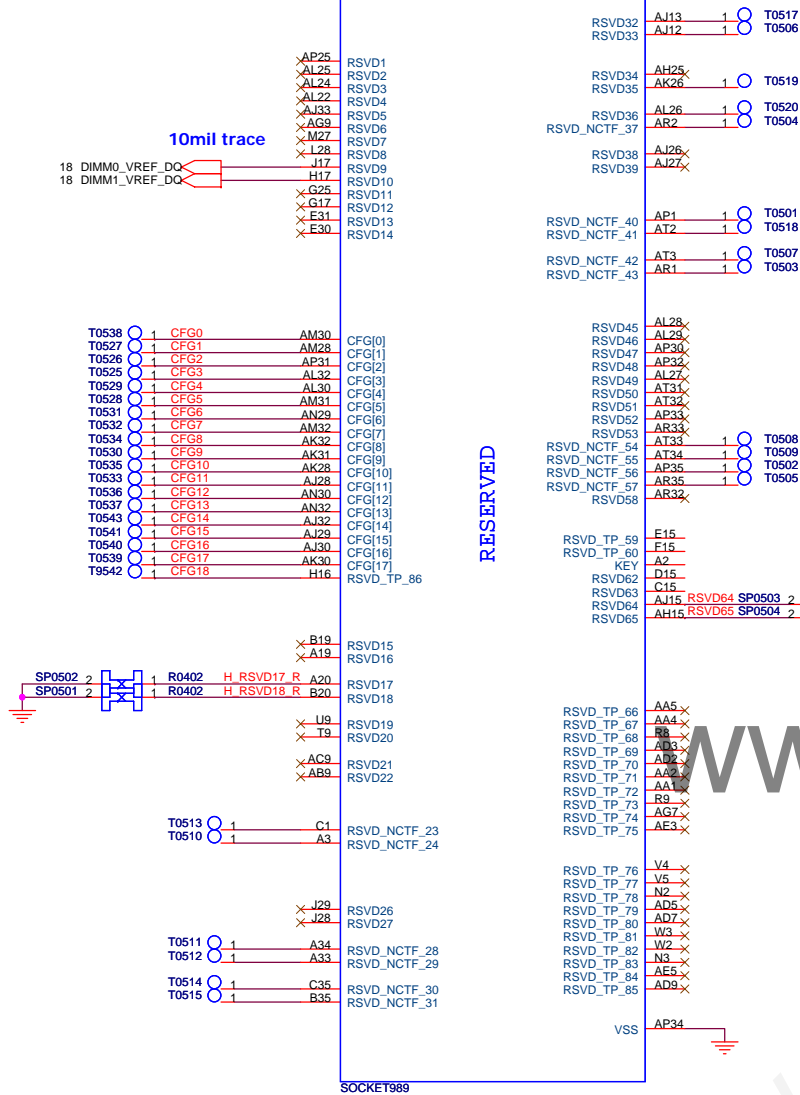
The wide of EXP_RBIAS is 20mils.



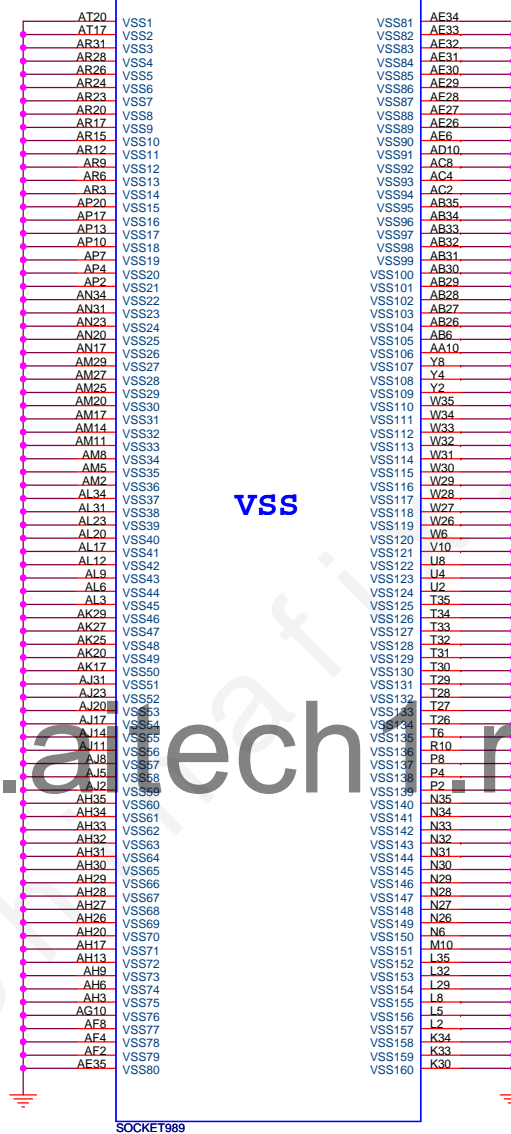
PEGATRON		Title : CPU(1)_DMI,PEG	
		Engineer: Peter Lo	
Size Custom	Project Name H24Y	Rev 1.0	
Date: Tuesday, April 06, 2010		Sheet 3 of 99	



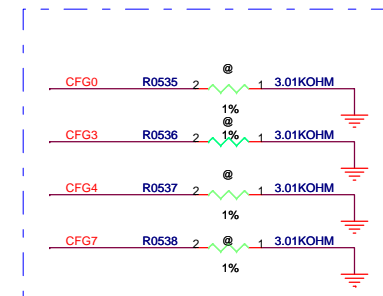
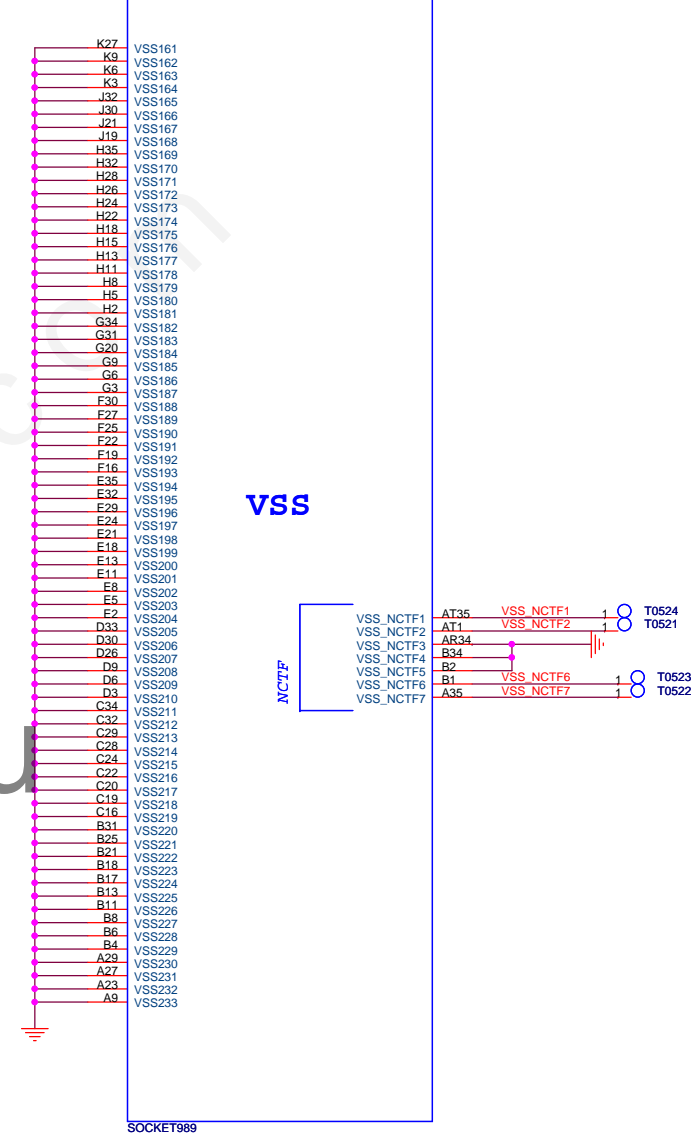
U0301E



U0301H



U0301I

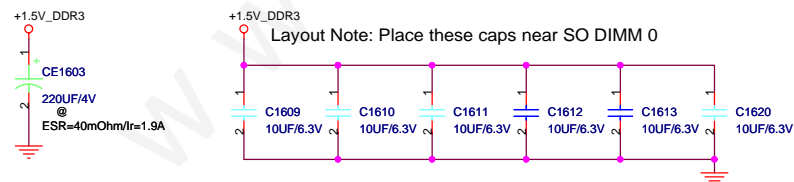
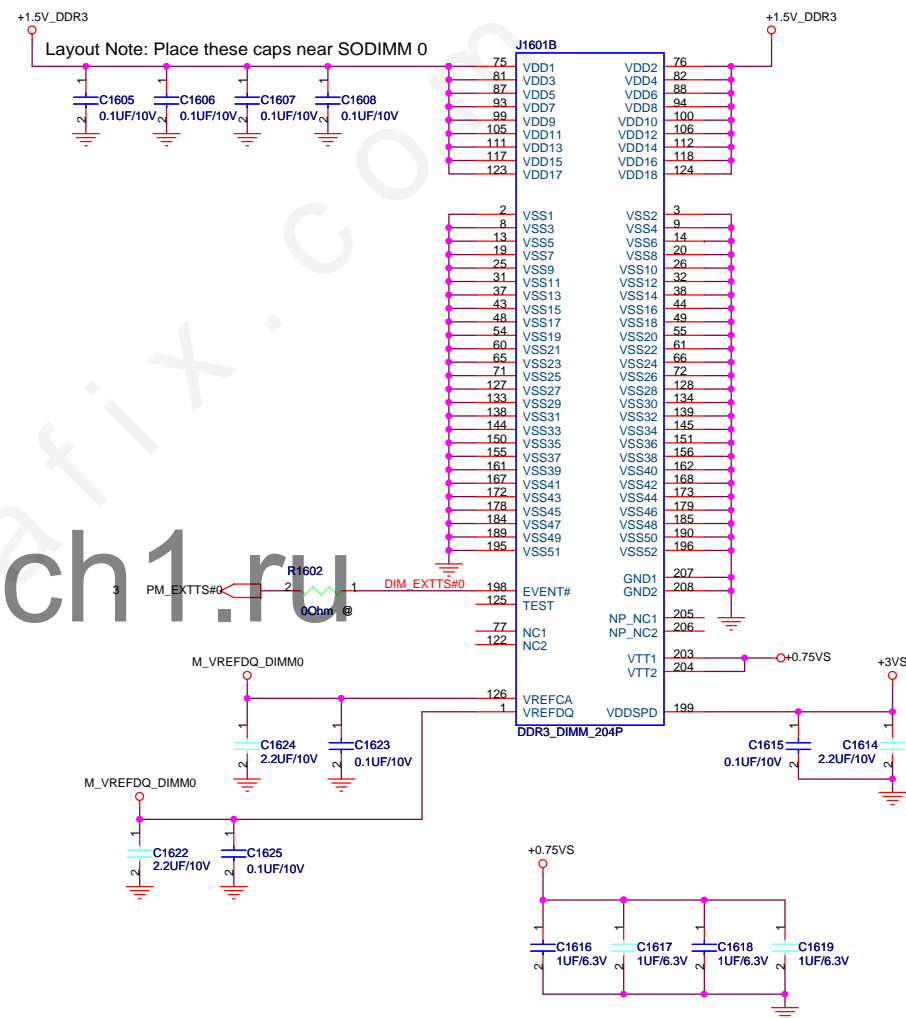
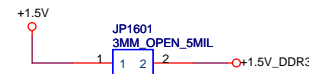


PEGATRON Title : CPU(3)_CFG.GND
Engineer: Peter Lo

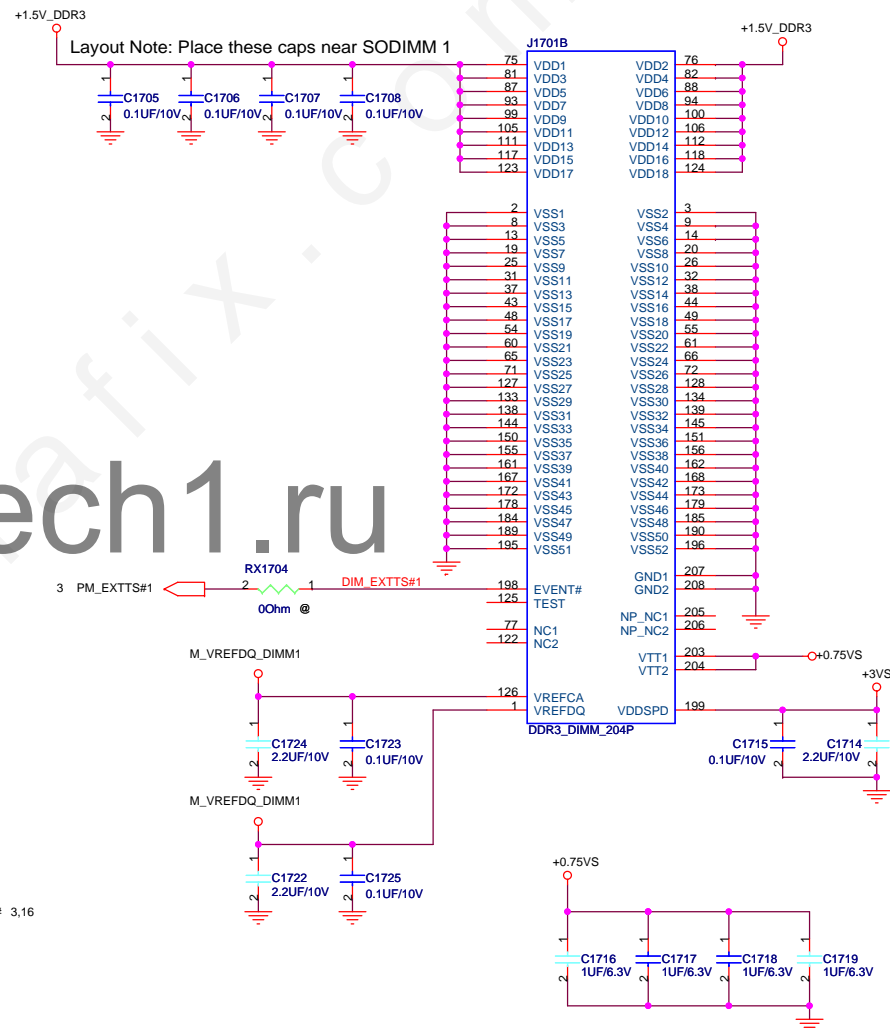
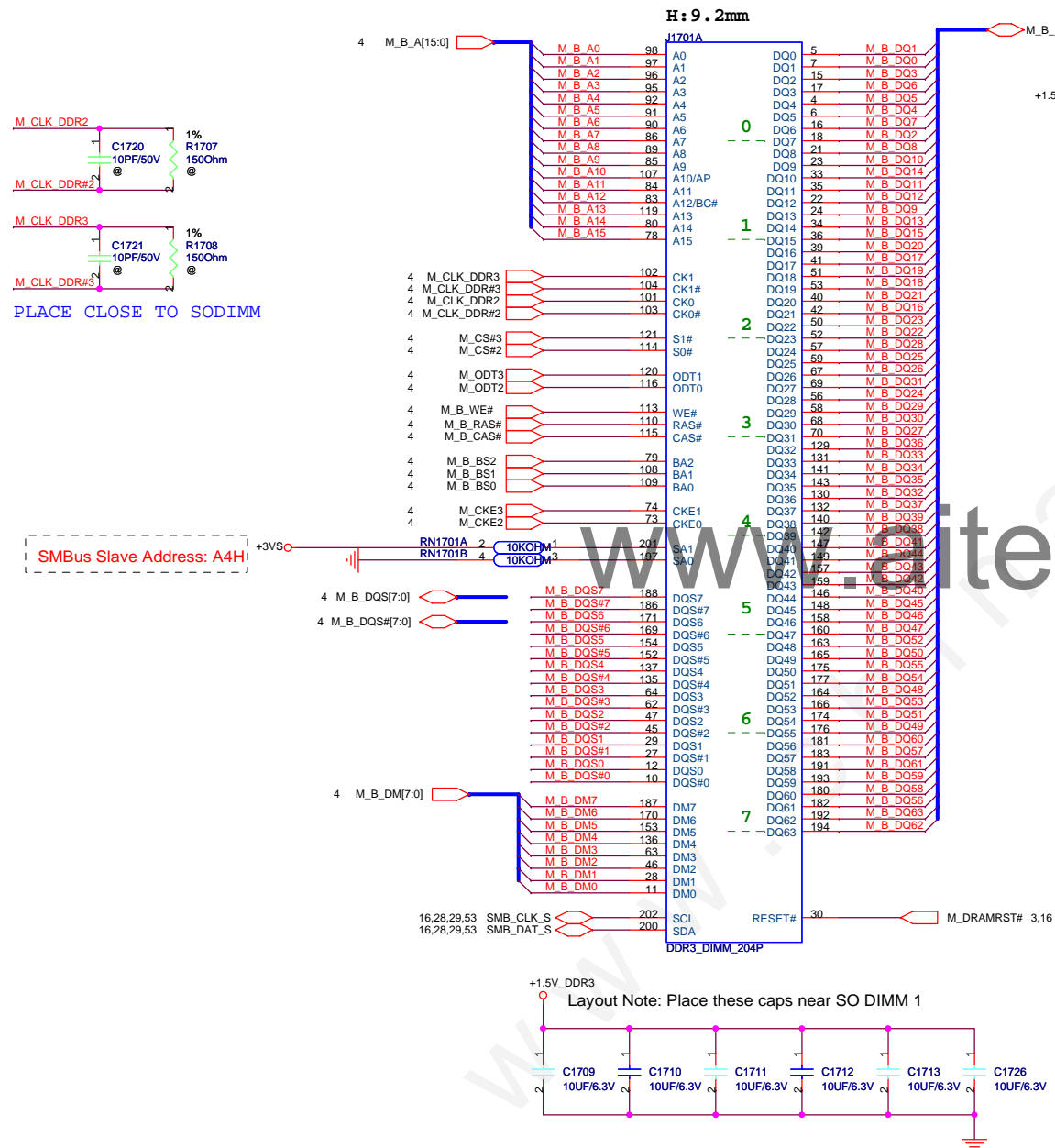
Size	Project Name	Rev
Custom	H24Y	1.0
Date: Tuesday, April 06, 2010	Sheet 5 of 99	

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PEGATRON		Title : HDMI Level Shifter	
		Engineer: Peter Lo	
Size B	Project Name H24Y		Rev 1.0
Date: Friday, March 12, 2010		Sheet 7	of 99

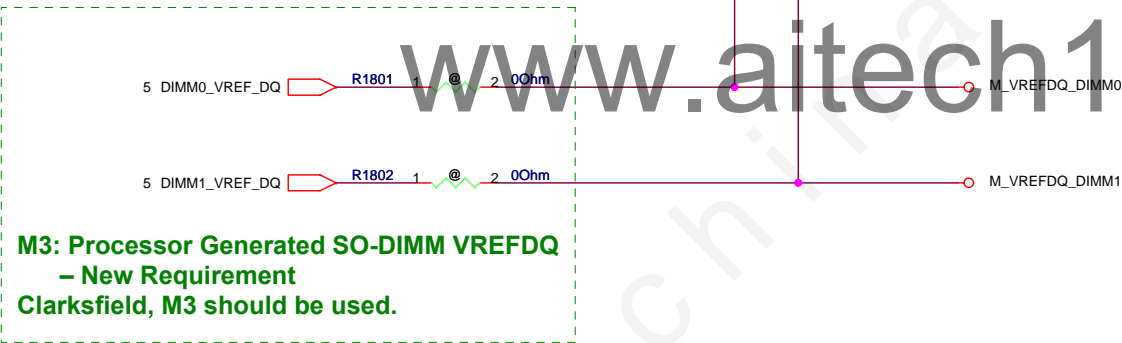
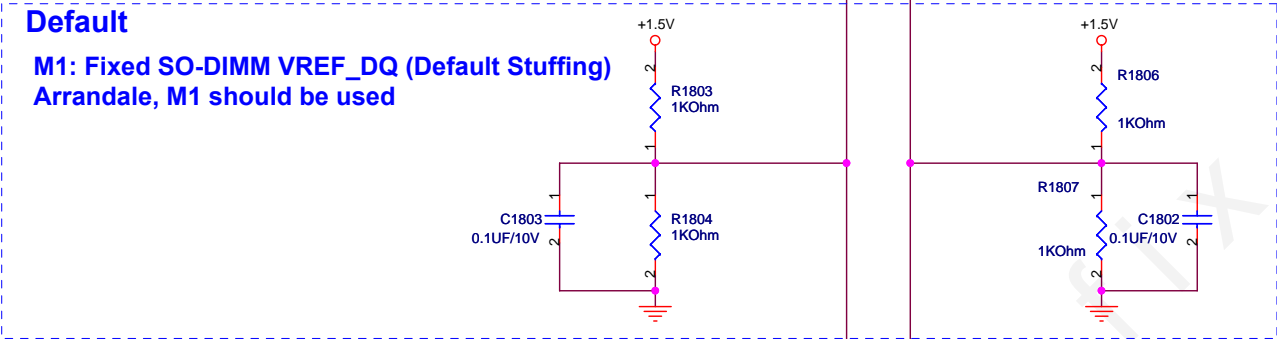


+1.5V +1.5V 6,16,18,57,83,91
+1.5V_DDR3 +1.5V_DDR3 16
+0.75VS +0.75VS 16,18,57,83
+3VS +3VS 3,16,20,21,22,23,24,25,26,27,28,29,30,31,32,43,45,46,50,51,53,56,57,61,66,80,86,91,92
M_VREFDQ_DIMM1 M_VREFDQ_DIMM1 16,18



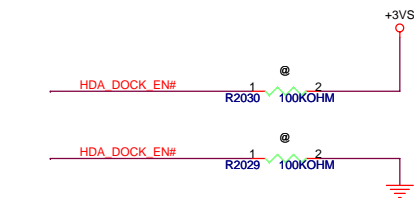
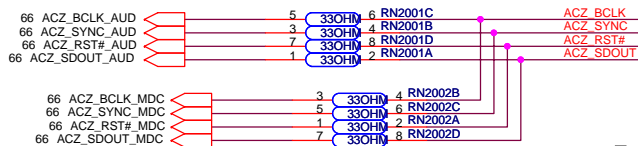
DDR3 Vref

+0.75VS		+0.75VS	16,17,57,83
+1.5V		+1.5V	6,16,57,83,91
M_VREFDQ_DIMM0		M_VREFDQ_DIMM0	16,17
M_VREFDQ_DIMM1		M_VREFDQ_DIMM1	16,17



CMOS Settings	JRST2001
Clear CMOS	Shunt
Keep CMOS	Open (Default)

TPM Settings	JRST2002
Clear ME RTC Registers	Shunt
Keep ME RTC Registers	Open (Default)



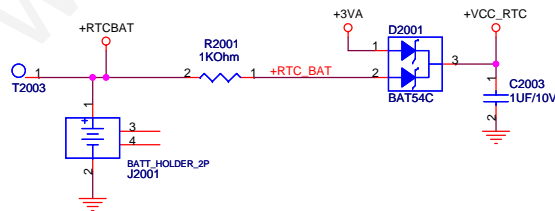
Strap information:

HDA_SPKR: No reboot strap
Low: Disable.
High: Enable

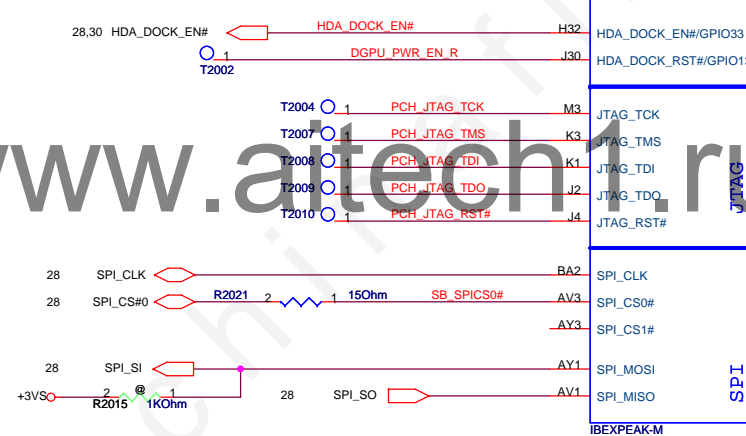
HDA_DOCK_EN#:
1. Flash descriptor security:
Sampled low: override
Sampled high: in effect.
2. GPIO33 low on the rising edge of PWROK,
Will also disable Intel MR.

SPI_MOSI: iTPM strap.
Mount R2015: Enable
Unmount R2015: Disable(default)

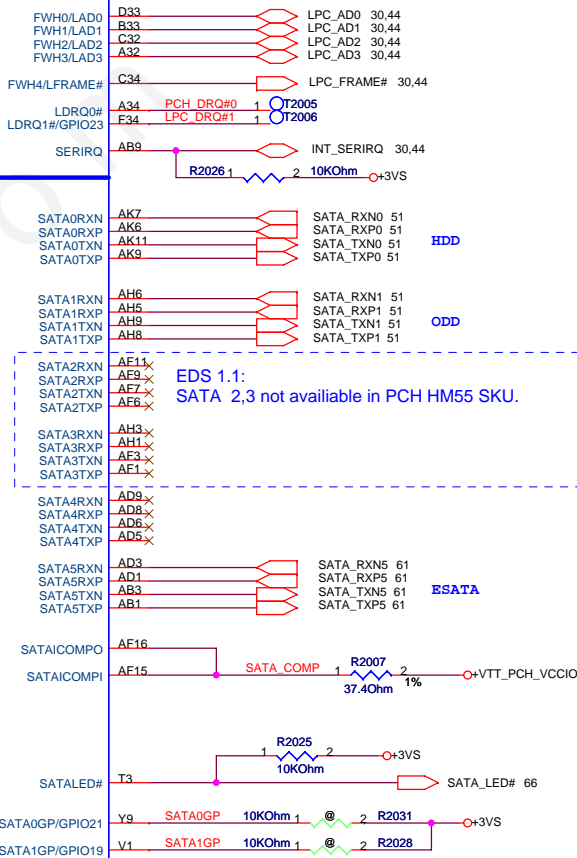
RTC battery



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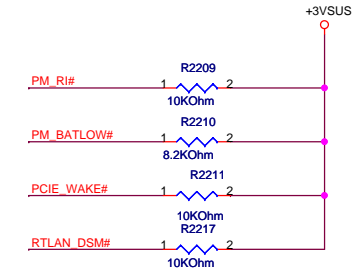
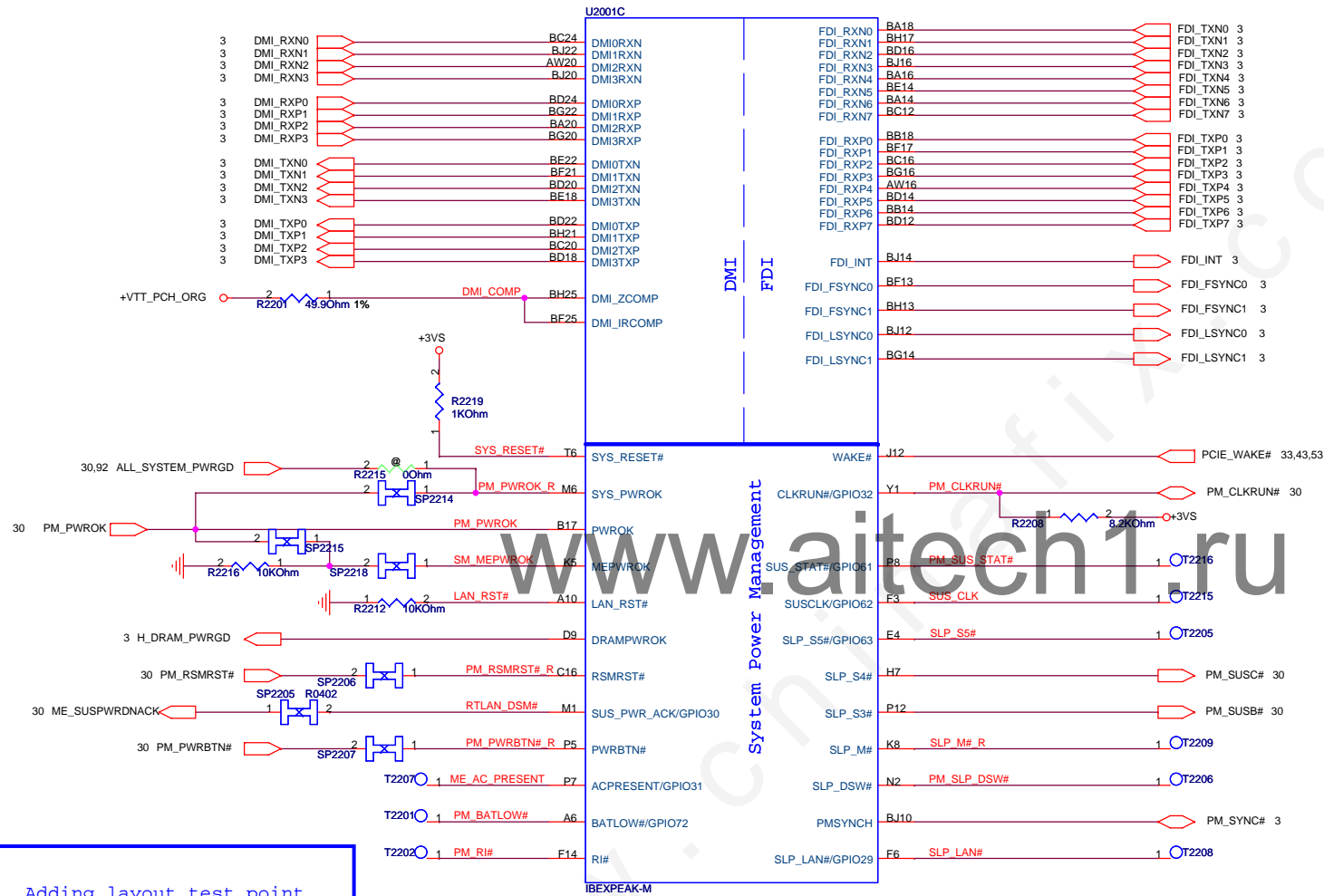
+3VS \rightarrow +3VS 3,16,17,21,22,23,24,25,26,27,28,29,30,31,32
+VTT_PCH_VCCIO \rightarrow +VTT_PCH_VCCIO 26,27
+VCC_RTC \rightarrow +VCC_RTC 27



EDS 1.1:
SATA_2,3 not available in PCH HM55 SKU.

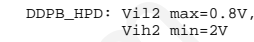
ESATA

+3VSUS  +3VSUS 21,24,25,27,30,33,34,43,56,66,81,90,92
+3VS  +3VS 3,16,17,20,21,23,24,25,26,27,28,29,30,31,32,43,45,46,50,51,53,56,57,61,66,80,86,91,92
+VTT_PCH_ORG  +VTT_PCH_ORG 21,26,27

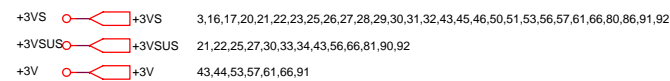


Adding layout test point
for boundary scan
2009/11/06

PM_RSMRST# R	1	T2210
PM_PWROK	1	T2211
SM_MEPWROK	1	T2212
LAN_RST#	1	T2213
PM_PWROK_R	1	T2214



Size Custom	Project Name H24Y	Rev 1.0
Date: Tuesday, April 06, 2010		Sheet 23 of 99



Boot BIOS Strap

PCI_GNT1#	PCI_GNT0#	Boot BIOS Location
0	0	LPC
0	1	Reserved
1	0	PCI
1	1	SPI (PCH)

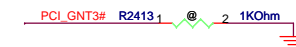
Sampled on rising edge of PWROK.



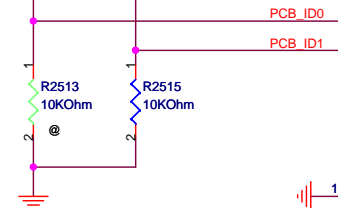
**GNT3#: A16 swap override Strap/
Top-Block swap override jumper**

Low=Enabled A16 swap override/
Top-Block swap override

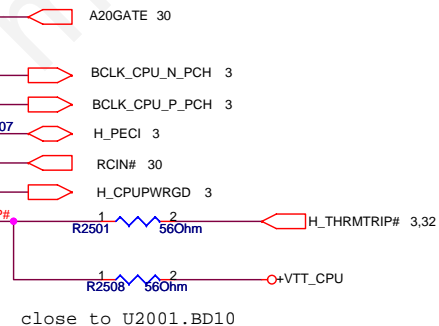
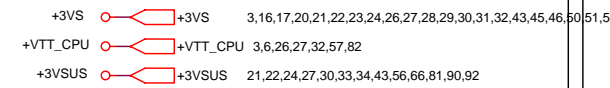
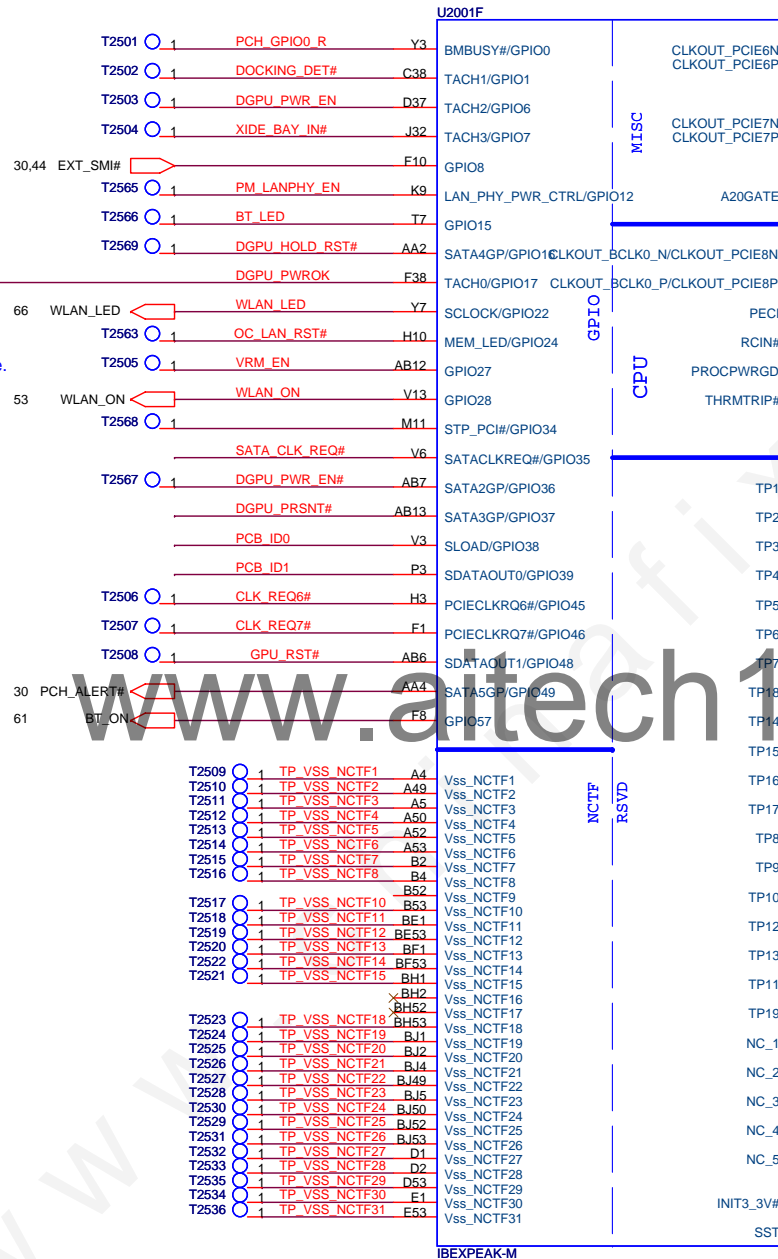
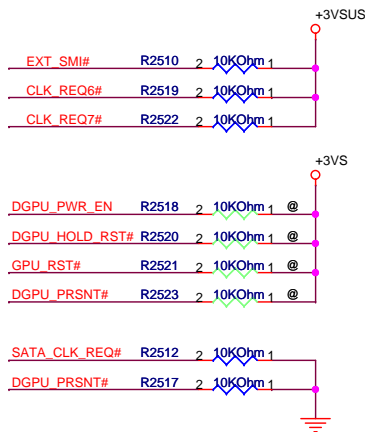
High=Default



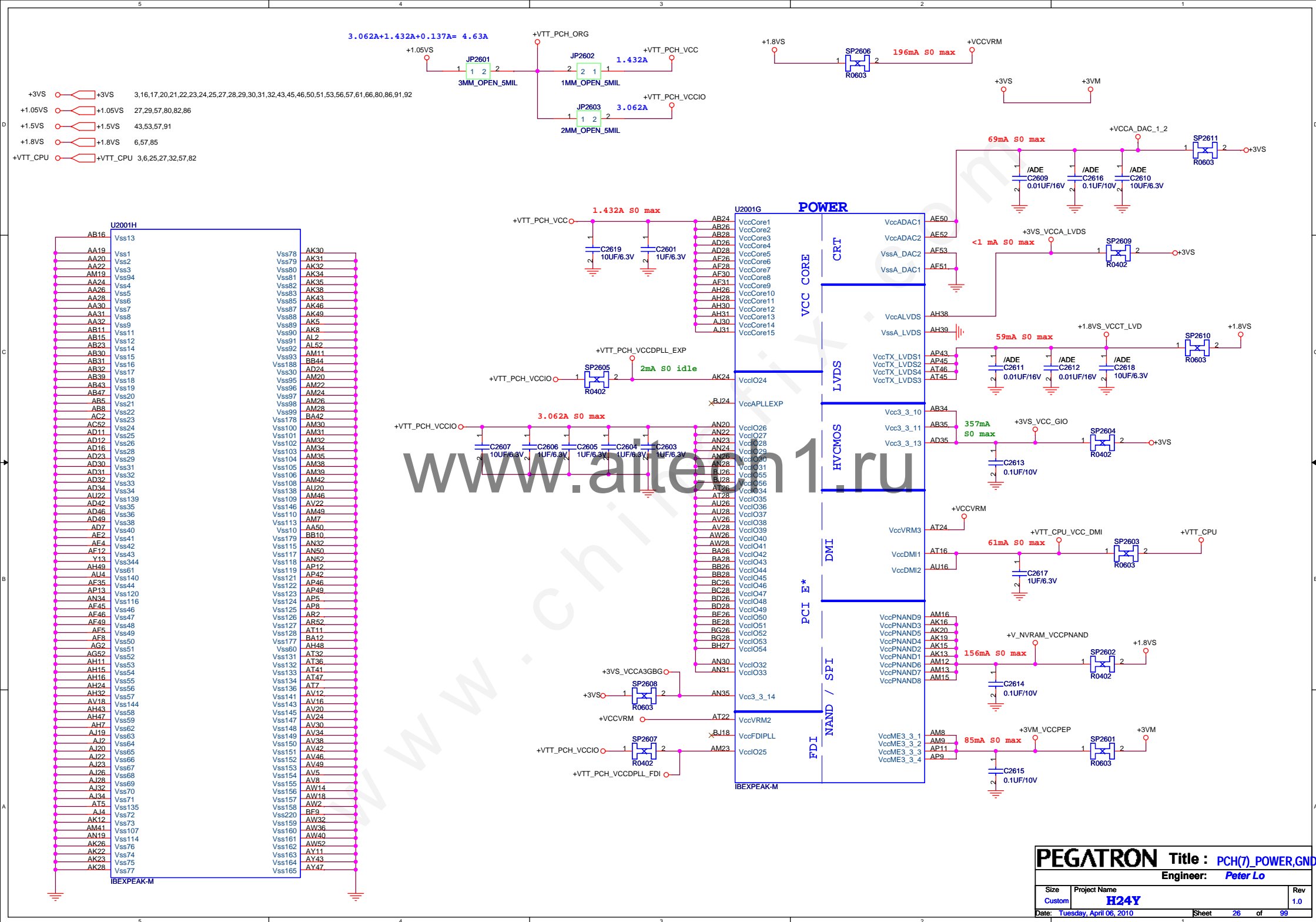
ID0	ID1	SKU
0	0	CFD non-iAMT
0	1	CFD iAMT
1	0	AUB non-iAMT
1	1	AUB iAMT

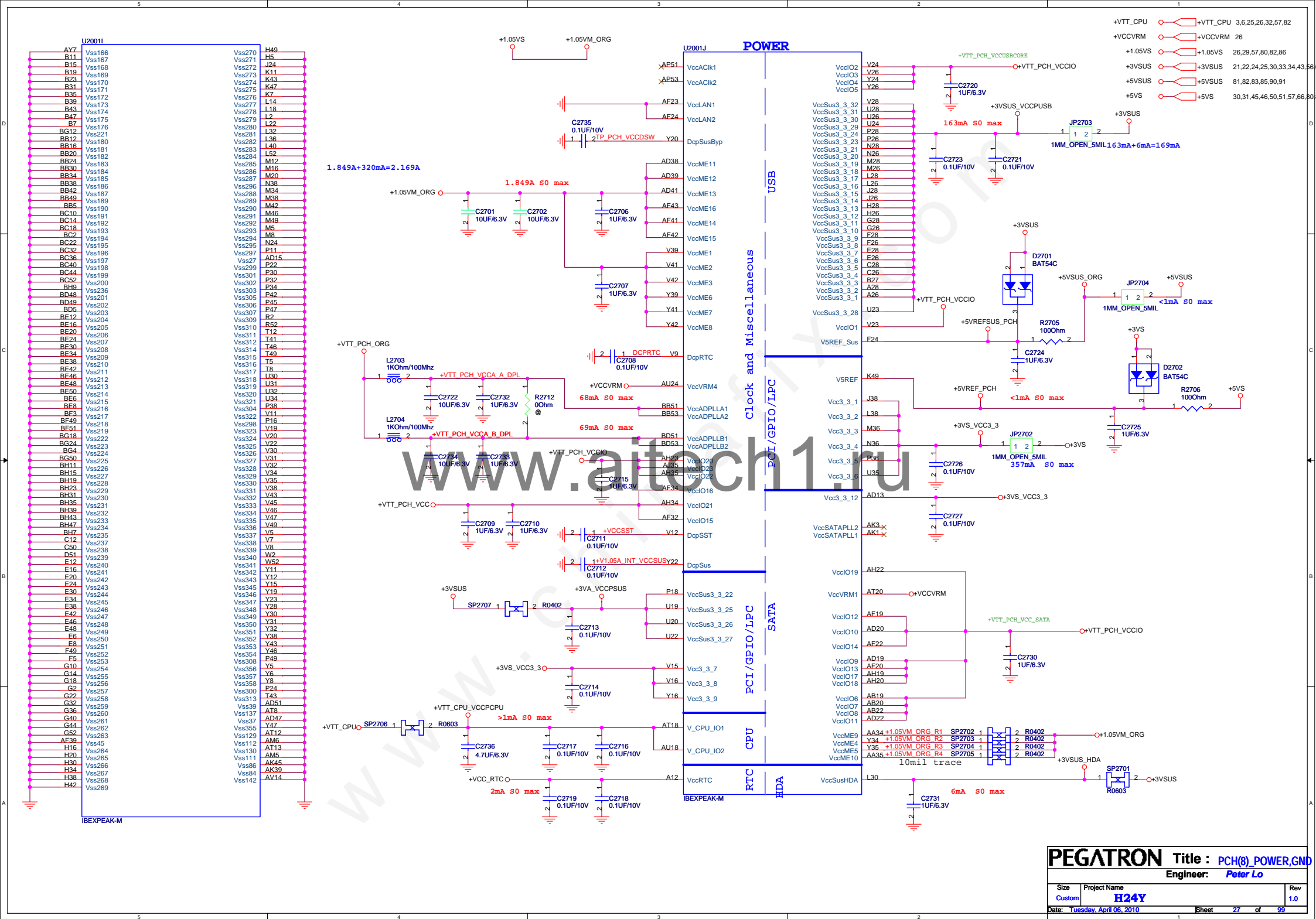


GPIO 27:Enable VCCVRM,Low=disable.
Default internal pull up.

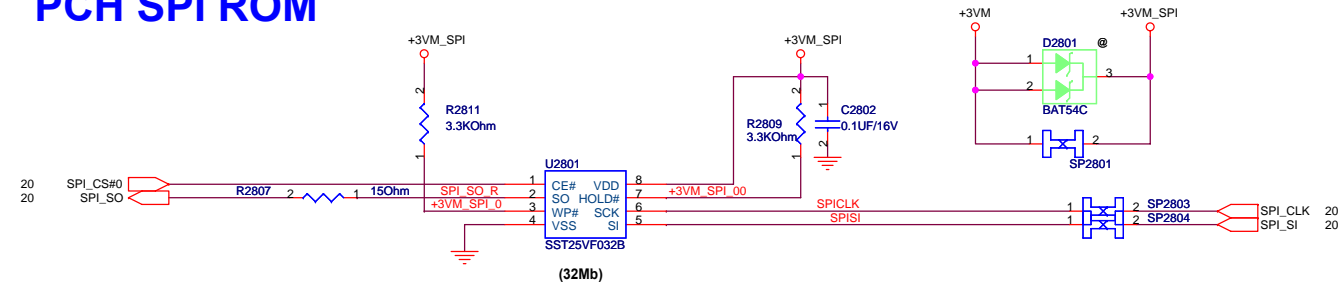


close to U2001.BD10

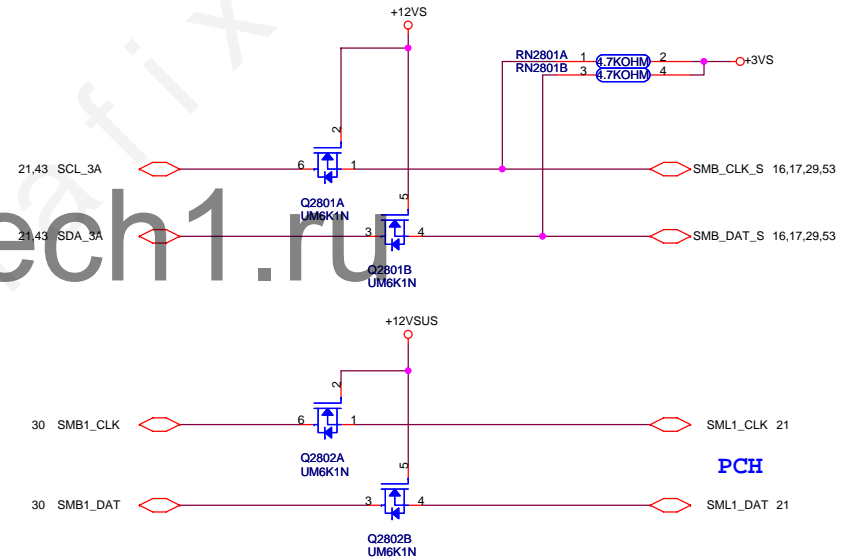
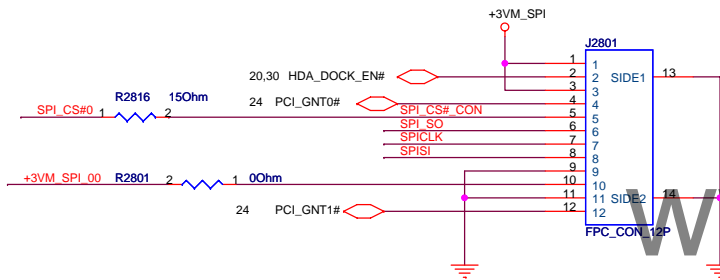




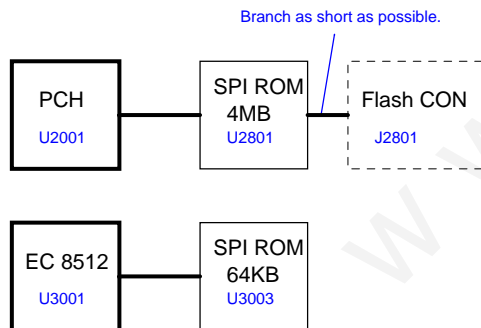
PCH SPI ROM



SMBUS Link device
DDR
CLKGEN
DEBUG
WLAN

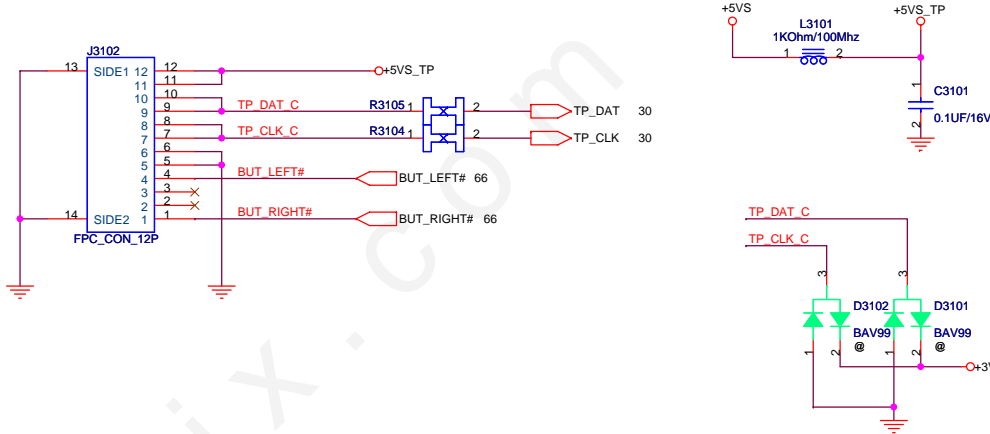


SPI Setting for layout:



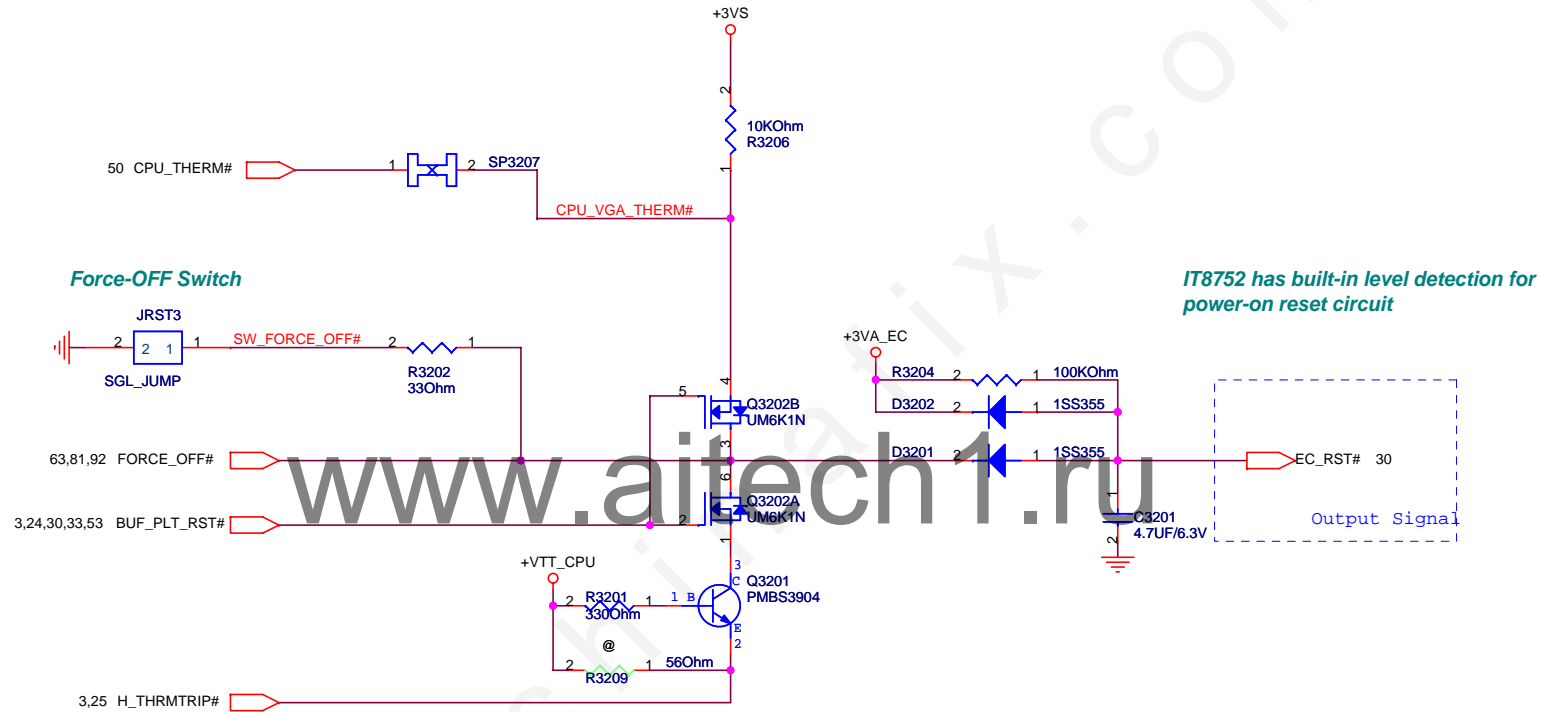
+3VA_EC	+3VA_EC	30,32
+3V	+3V	24,43,44,53,57,61,66,91
+3VS	+3VS	3,16,17,20,21,22,23,24,25,26,27,28,29,30,32,43,45,46,50,51,53,56,57,61,66,80,86,91,92
+5VA	+5VA	81,90
+5V	+5V	45,52,57,91
+5VS	+5VS	27,30,45,46,50,51,57,66,80,86,91

Touch Pad

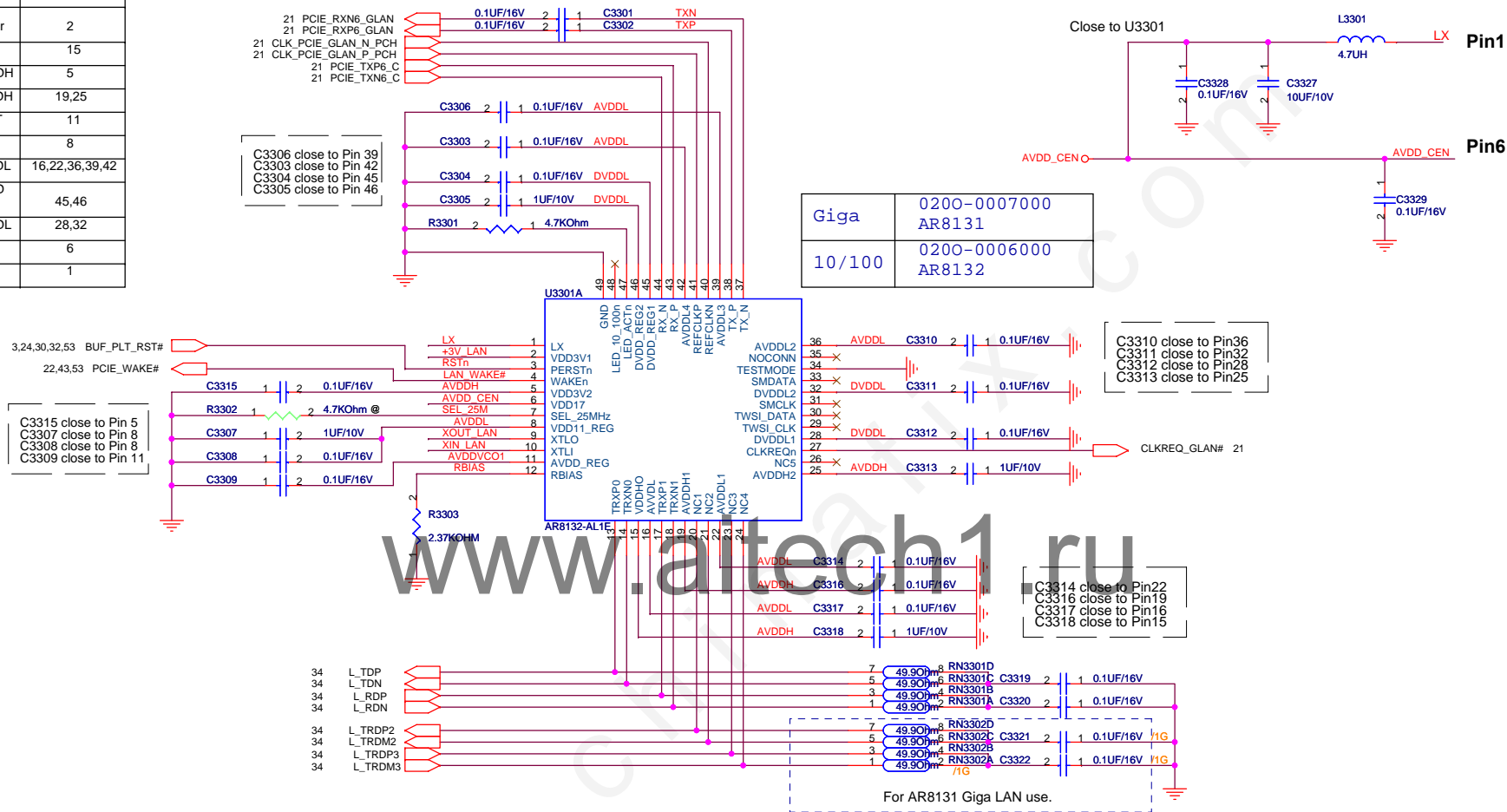


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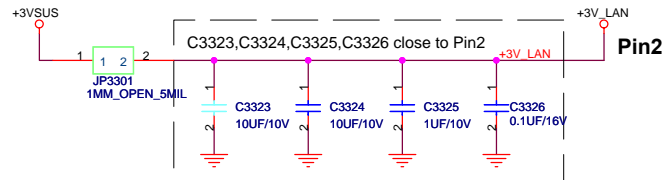
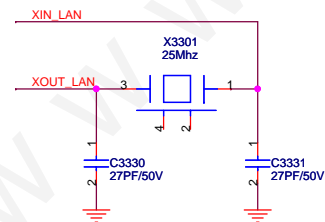
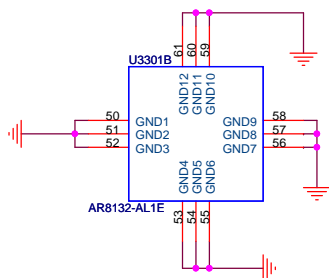
Thermal Policy



Power Table	PIN
3.3V Power	2
2.5V OUT	15
2.5V DVDDH	5
2.5V AVDDH	19,25
1.25V OUT	11
1.1V OUT	8
1.1V AVDDL	16,22,36,39,42
1.1V DVDD OUT	45,46
1.1V DVDDL	28,32
1.7V SWR	6
1.7V pin	1



Termination Resistor Place near LAN chip



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PEGATRON		Title : MDC	
		Engineer: Peter Lo	
Size	Project Name	Rev	
Custom	H24Y	1.0	
Date: Friday, March 12, 2010	Sheet 35 of 99		1

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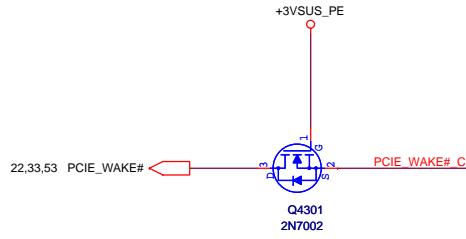
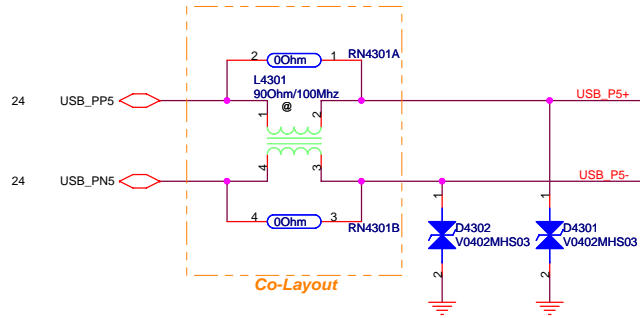
PEGATRON		Title : CODEC ALC269-VB	
		Engineer: Peter Lo	
Size C	Project Name H24Y	Rev 1.0	
Date: Friday, March 12, 2010		Sheet	36 of 99

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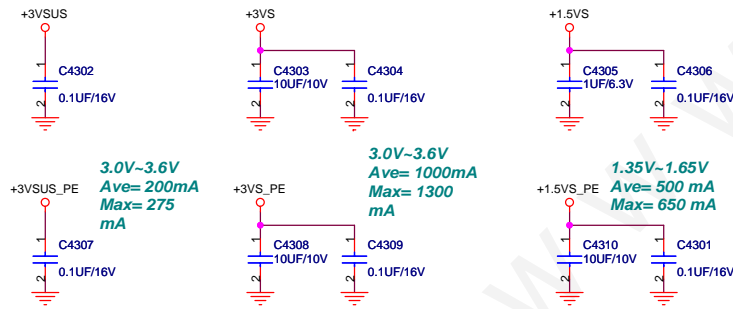
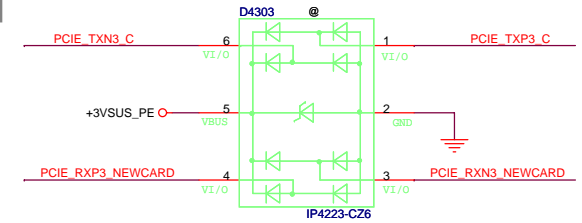
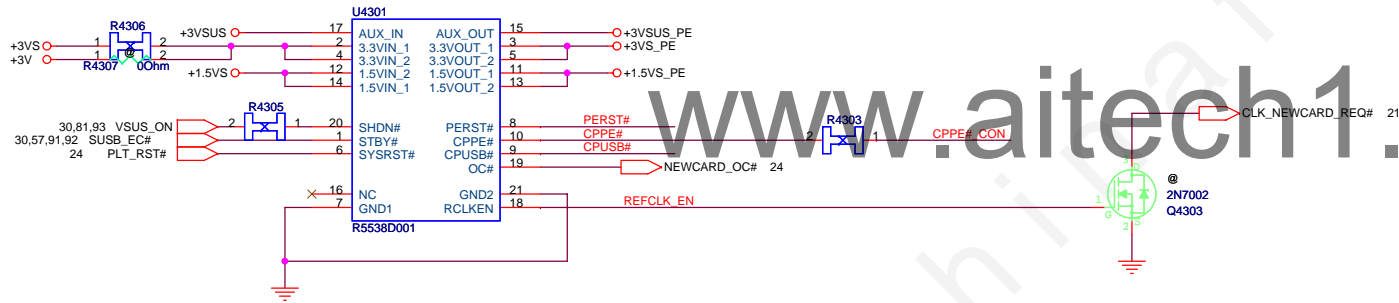
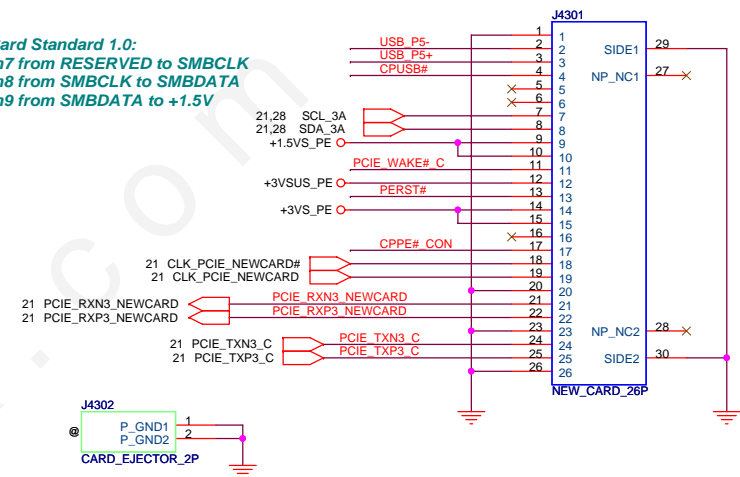
PEGATRON		Title : AMPLIFER & DEPOP	
		Engineer: Peter Lo	
Size C	Project Name H24Y	Rev 1.0	
Date: Friday, March 12, 2010		Sheet 37 of 95	

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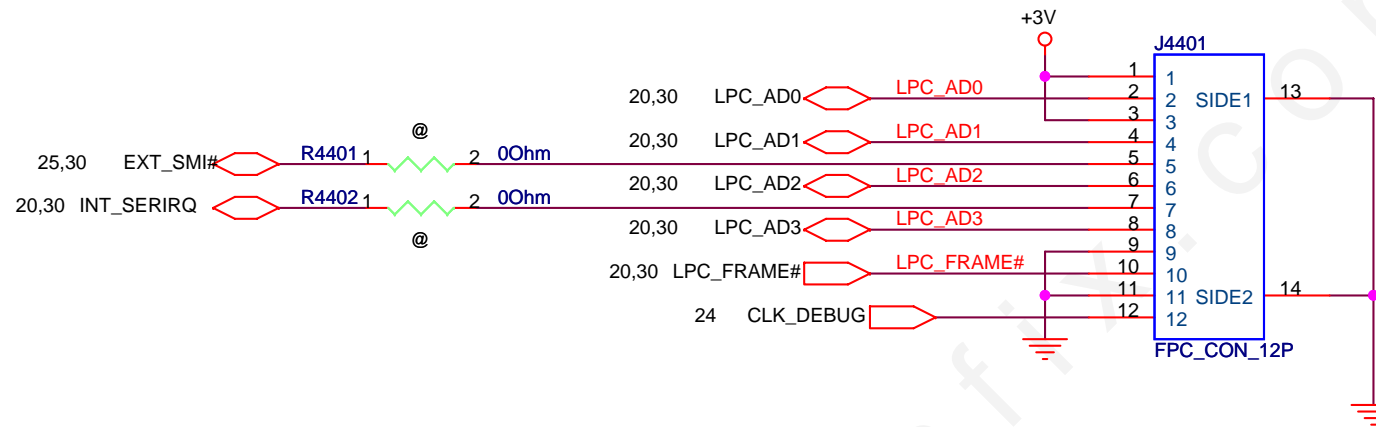
PEGATRON		Title : Cardreader_AU6433	
		Engineer: Peter Lo	
Size	Project Name		Rev
Custom	H24Y		1.0
Date: Friday, March 12, 2010		Sheet	40 of 99



!! ExpressCard Standard 1.0:
Change Pin7 from RESERVED to SMBCLK
Change Pin8 from SMBCLK to SMBDATA
Change Pin9 from SMBDATA to +1.5V

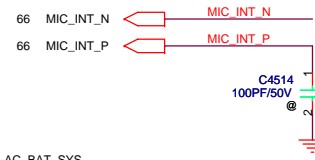
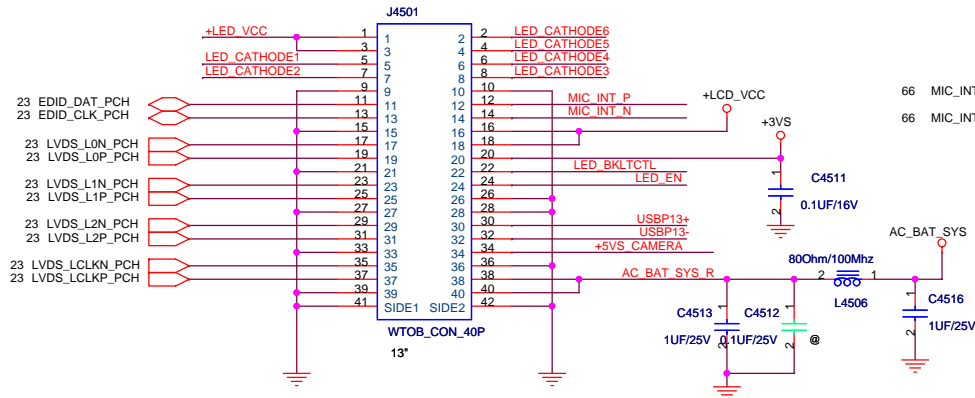


LPC Debug Port

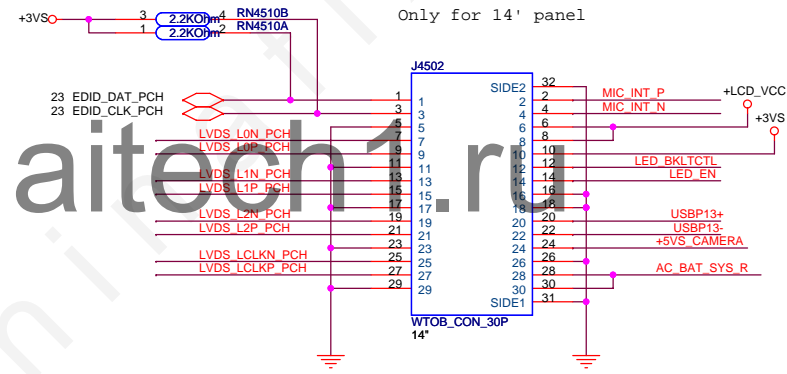
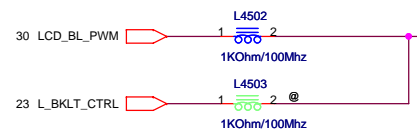
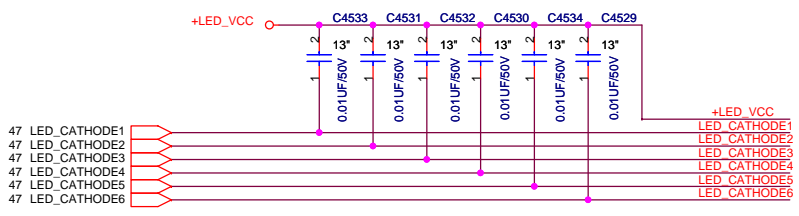
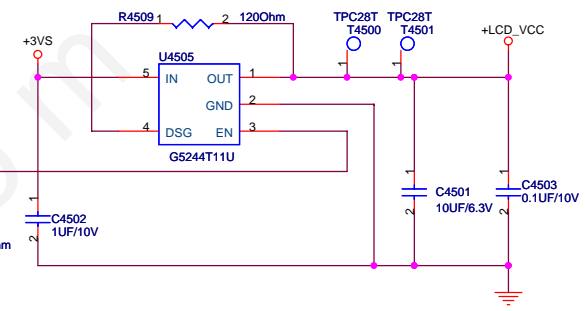


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PEGATRON		Title : BUG_Debug	
BG1VHW1		Engineer: Peter Lo	
Size A	Project Name H24Y		Rev 1.0
Date: Tuesday, April 06, 2010		Sheet 44 of 99	



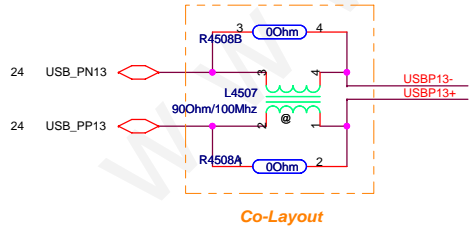
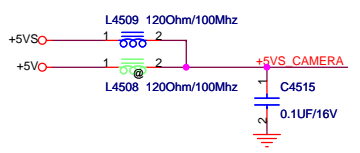
Power Switch for LCD Power



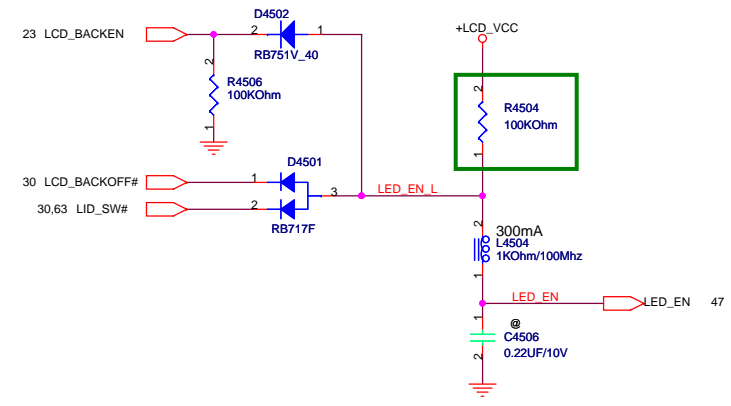
Only for 14' panel

For 14' panel
unmount J4501, C4529, C4530,
C4531, C4532, C4533, C4534
R4504 use 100KOhm

For 13' panel
unmount J4502
R4504 use 1KOhm



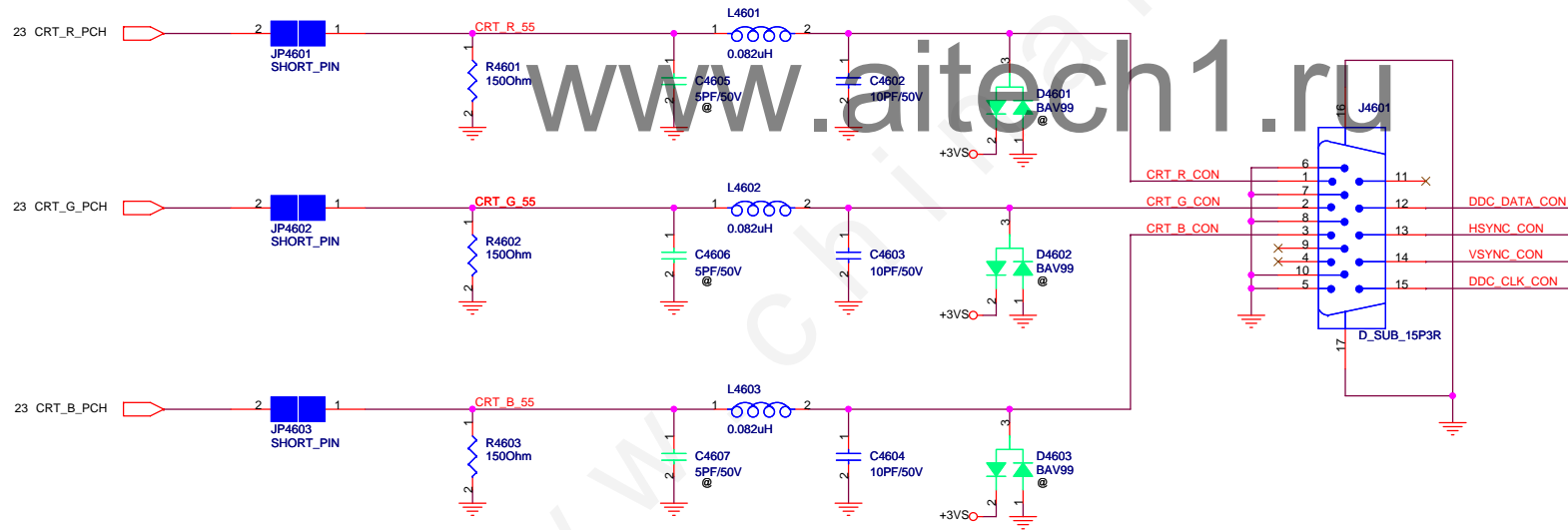
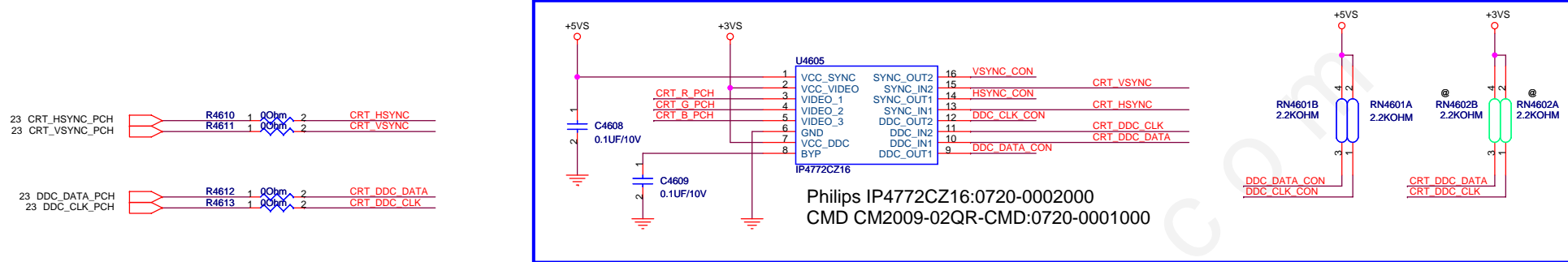
Co-Layout



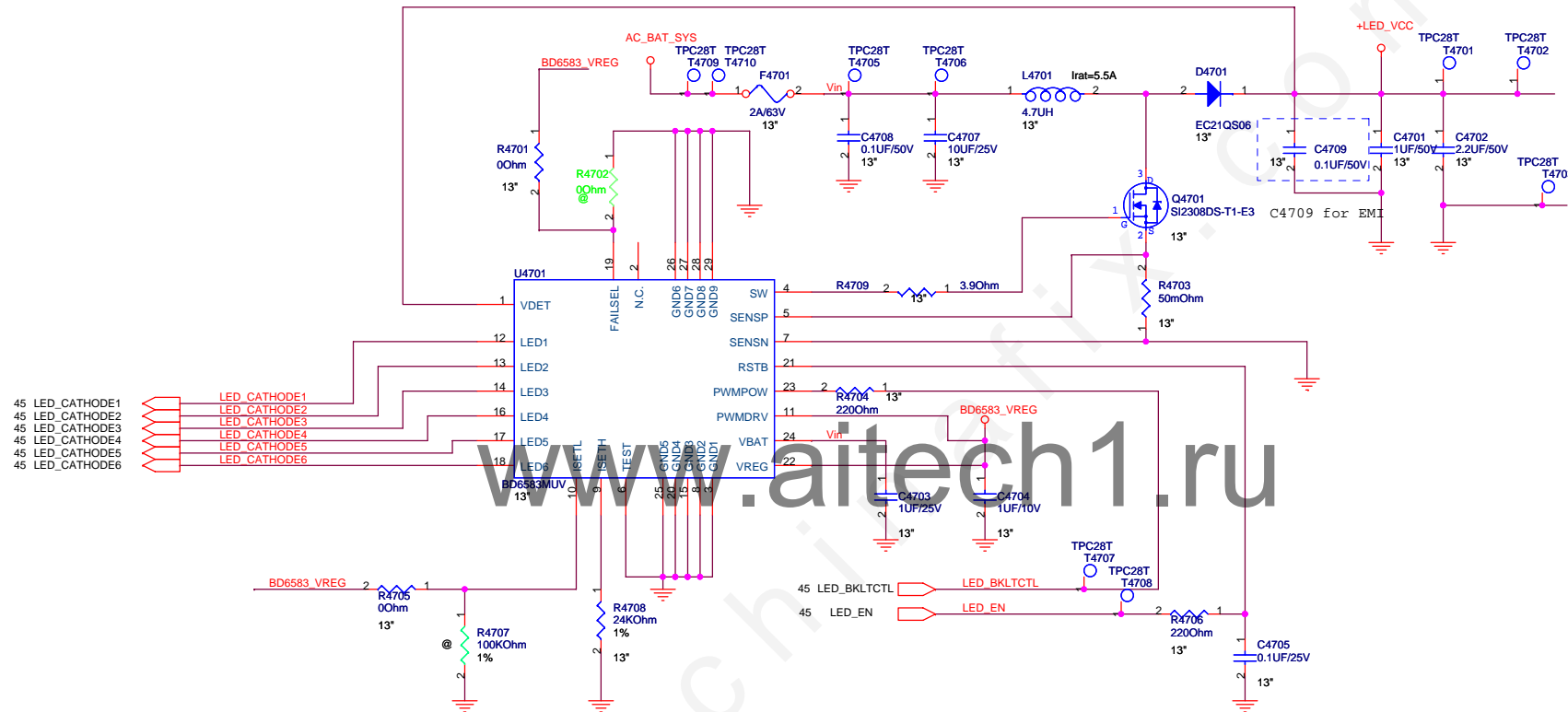
For non-Switchable Gfx

For iGPU

PLACE ESD IC near J4601

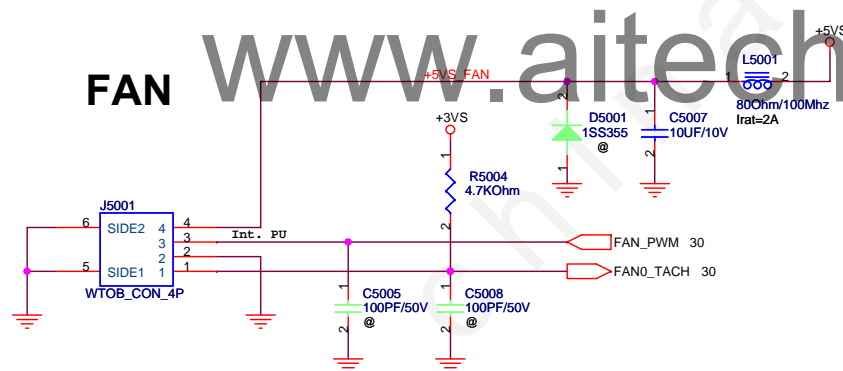
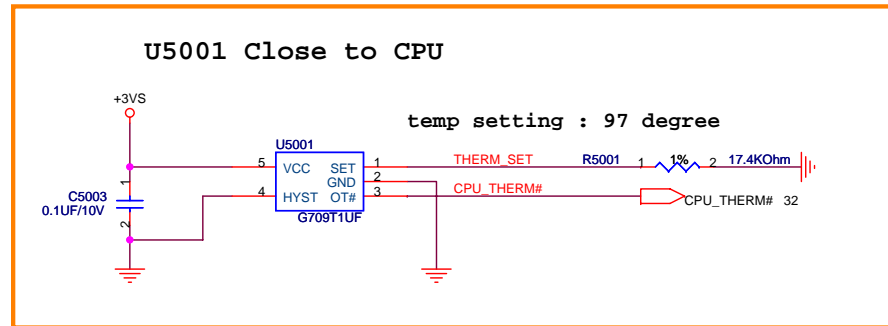


only for 13' panel

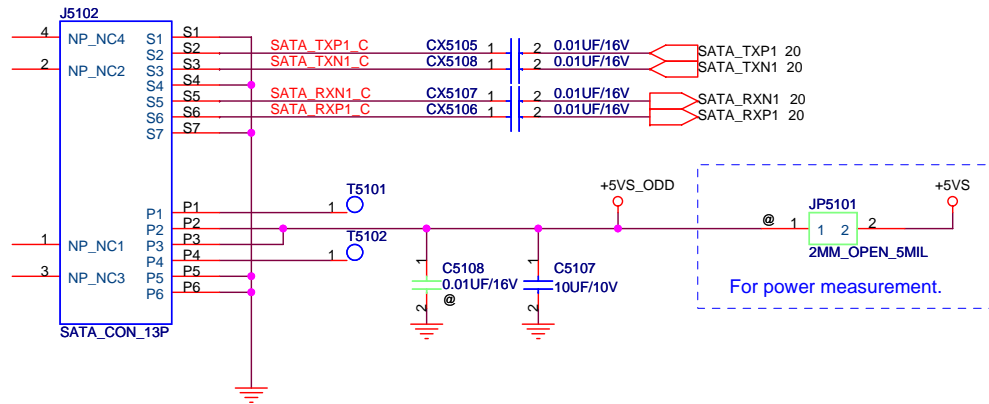


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PEGATRON		Title : TV(1)_HDMI	
		Engineer: Peter Lo	
Size	Project Name		Rev
C	H24Y		1.0
Date: Friday, March 12, 2010		Sheet	48 of 99

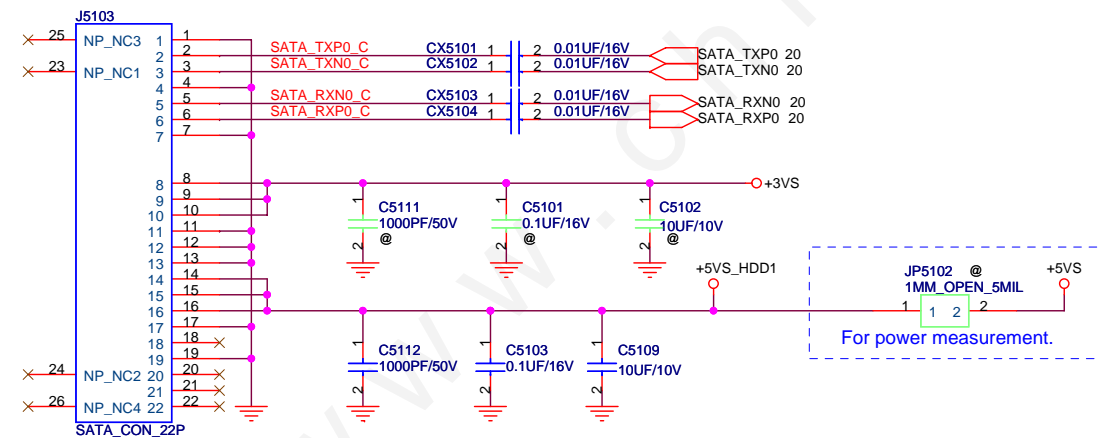


ODD CONN



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HDD CONN



PEGATRON Title : **XDD_HDD_ODD**

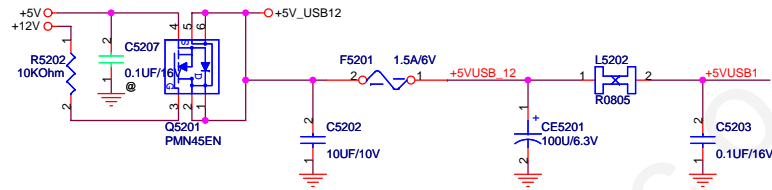
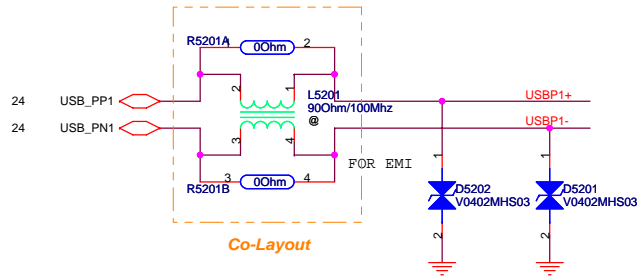
Engineer: **Peter Lo**

Size	Project Name	Rev
Custom	H24Y	1.0

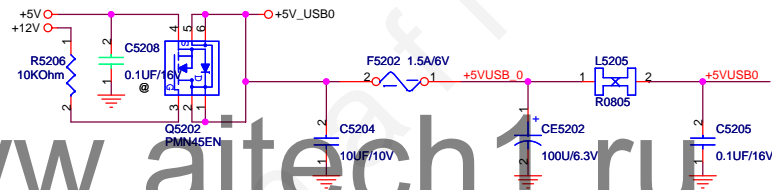
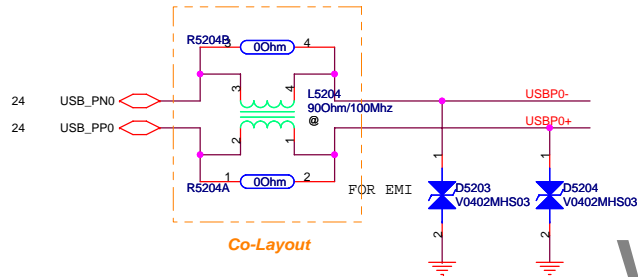
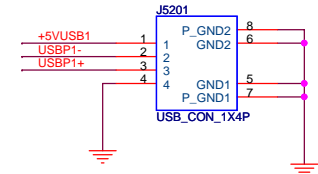
Date: Tuesday, April 06, 2010

Sheet 51 of 99

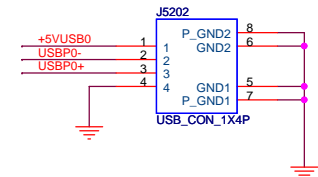
+5V → +5V 45,57,91



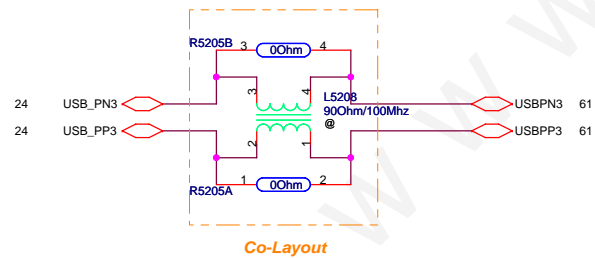
USB



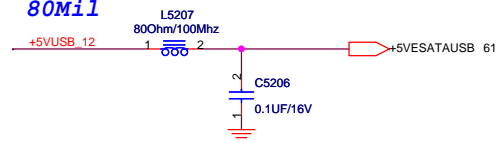
USB



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80mil



PEGATRON Title : **USB PORTS**

BU1-RD Div.1-HW RD Dept.3 Engineer: **Peter Lo**

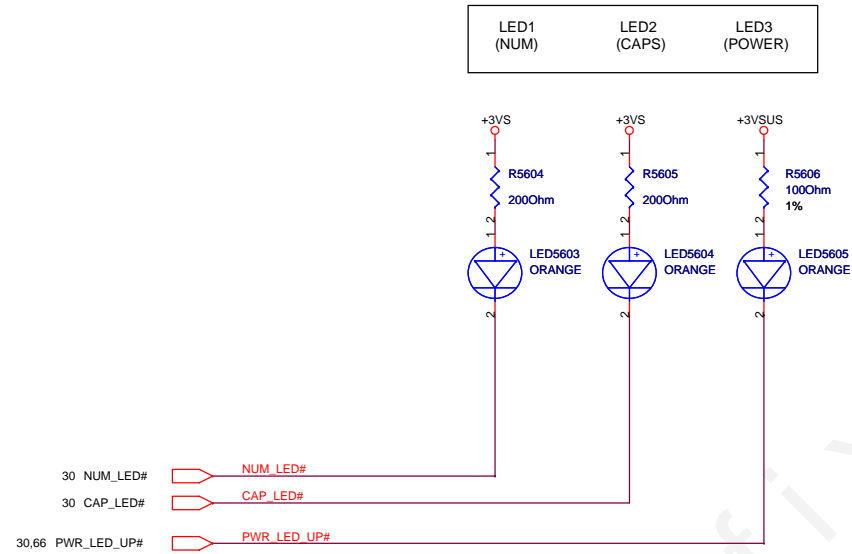
Size Project Name
Custom **H24Y**

Date: Tuesday, April 06, 2010 Sheet 52 of 99 Rev 1.0

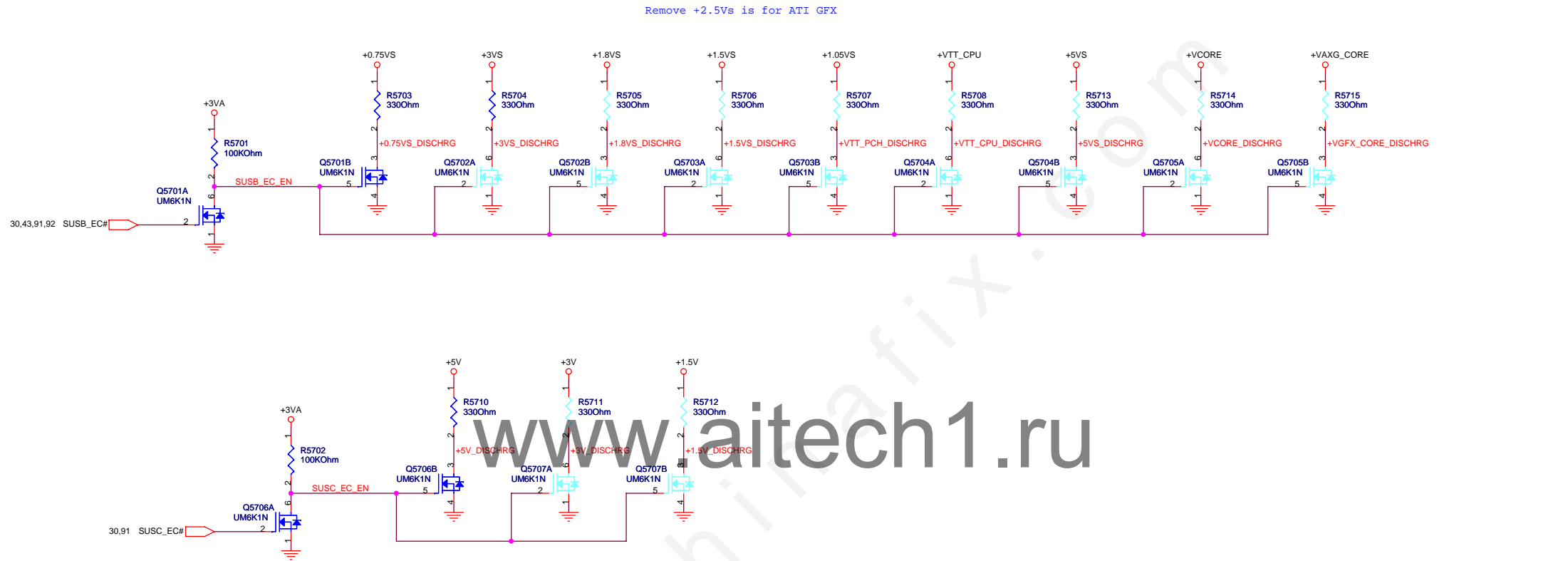
www.aitech1.ru

PEGATRON		Title : Camera / DMIC	
		Engineer: Peter Lo	
Size Custom	Project Name H24Y		Rev 1.0
Date: Friday, March 12, 2010		Sheet 54 of 99	1

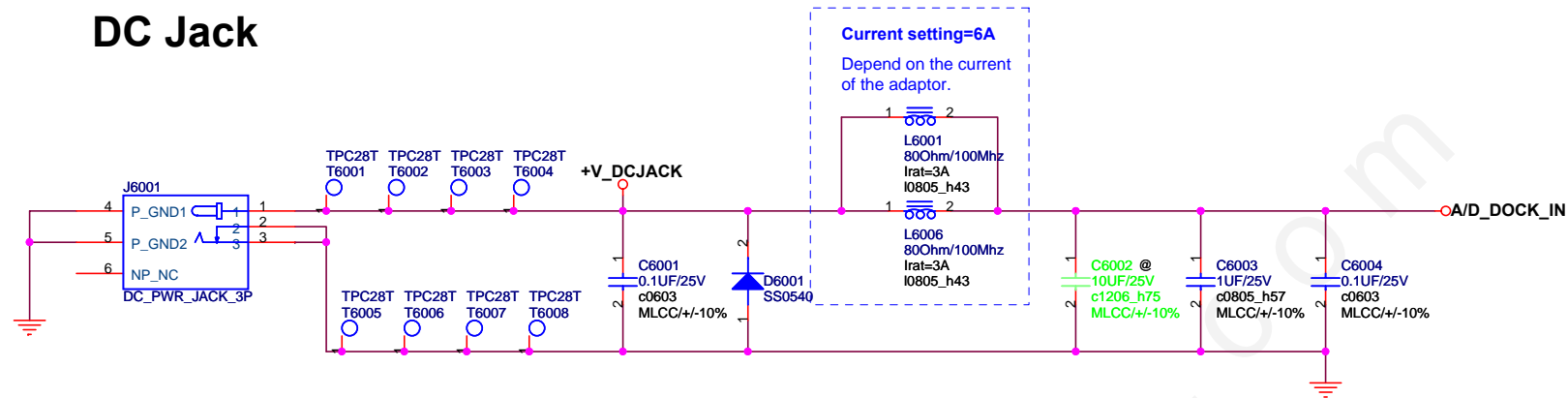
LED



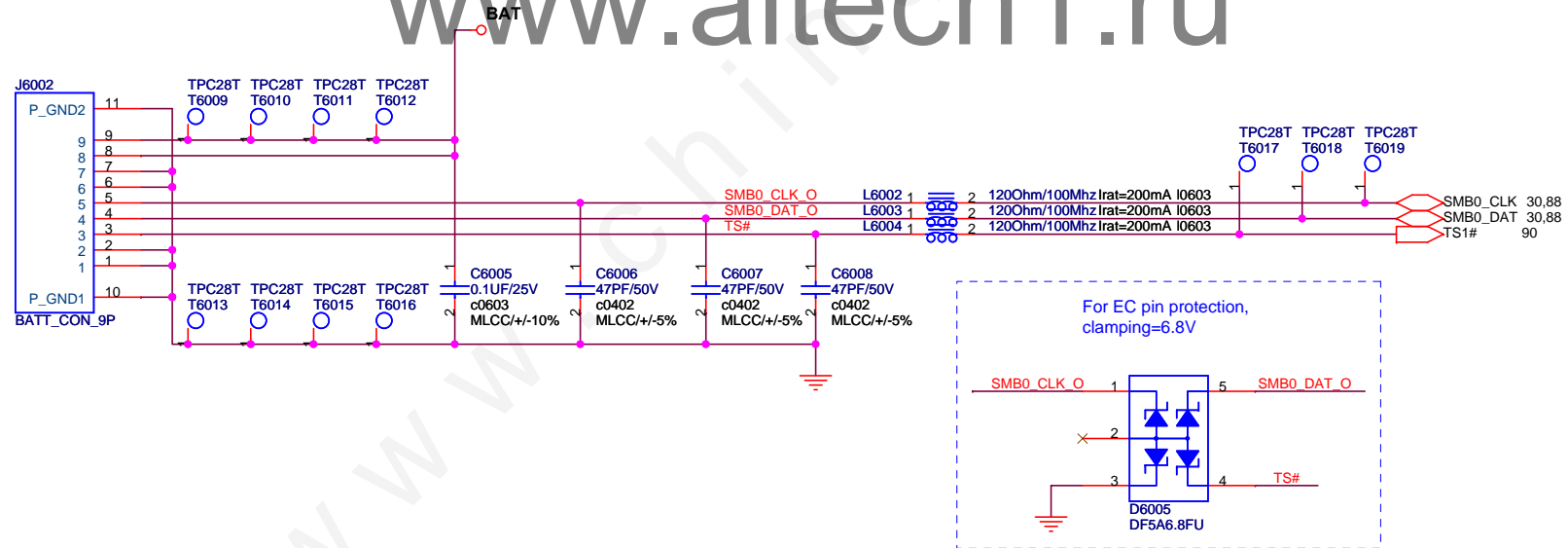
www.aitech1.ru



DC Jack



Battery Connector



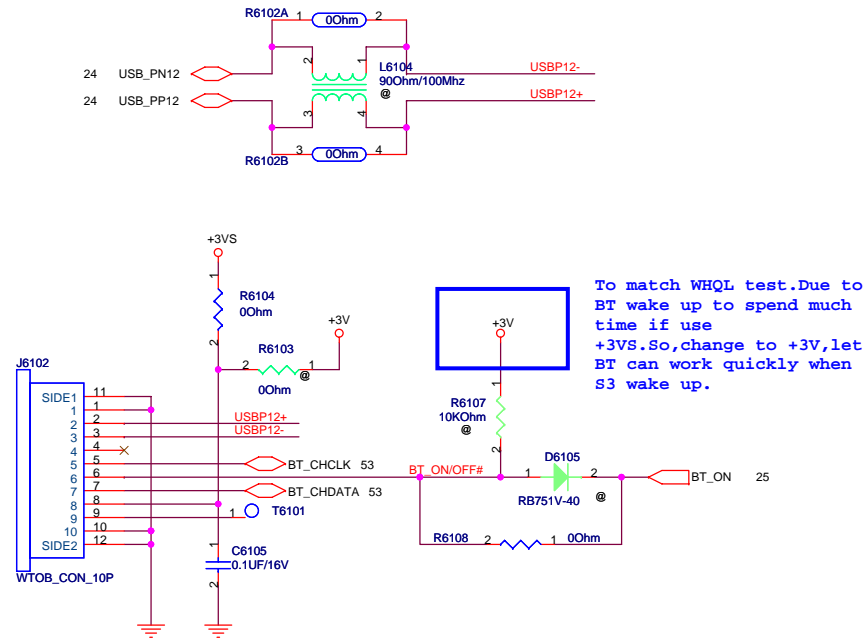
PEGATRON Title : DC_DC/BAT CONN

Engineer: Peter Lo

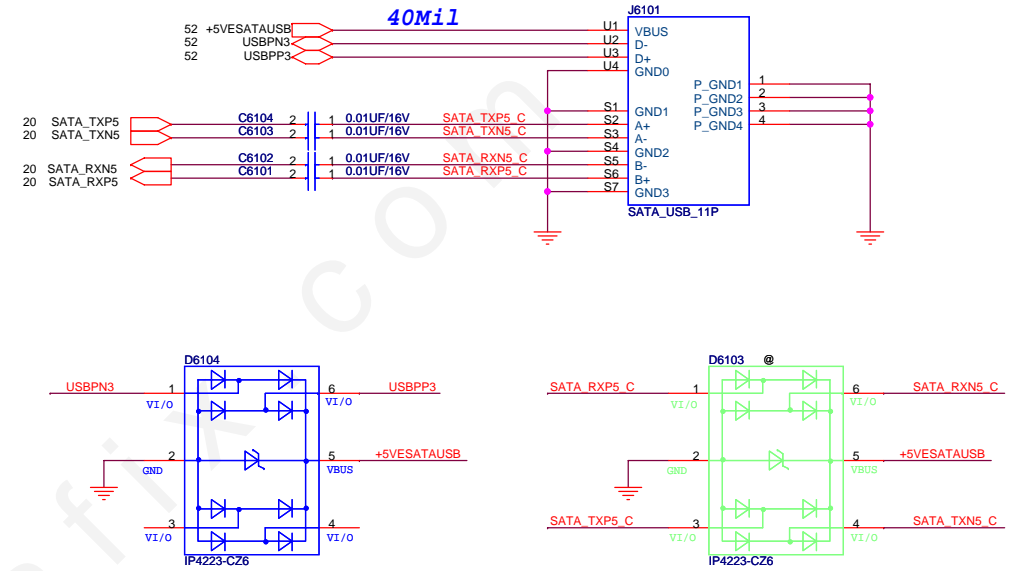
Size	Project Name	Rev
Custom	H24Y	1.0

Date: Tuesday, April 06, 2010 Sheet 60 of 99

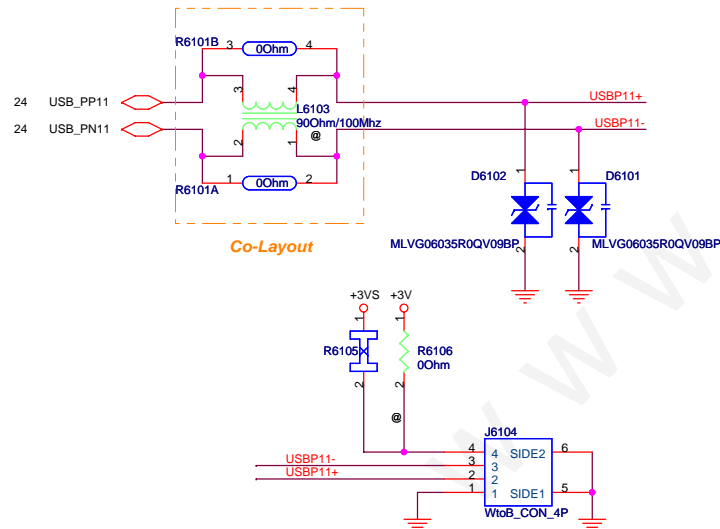
Bluetooth



E-SATA



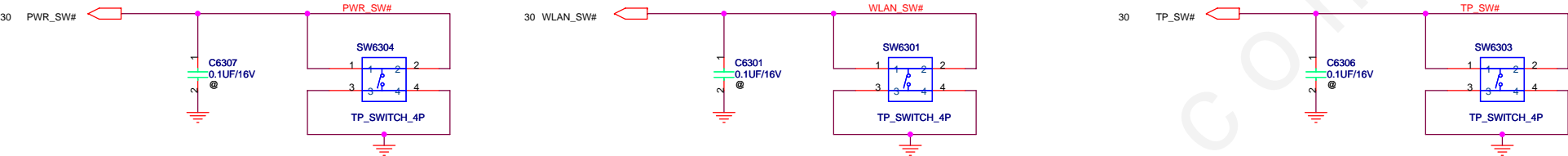
Fingerprint



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PEGATRON		Title : TPM	
		Engineer: Peter Lo	
Size A	Project Name H24Y		Rev 1.0
Date: Friday, March 12, 2010		Sheet	62 of 99

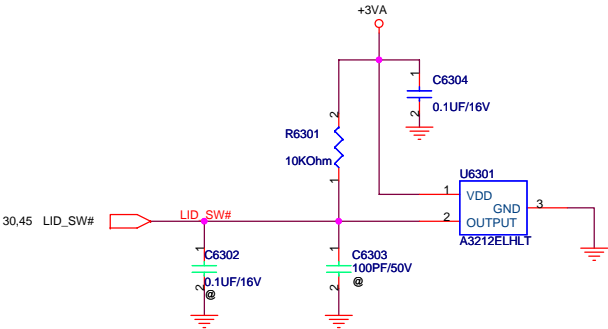
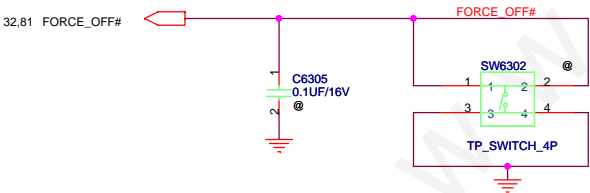
SWITCH (TOP SIDE)

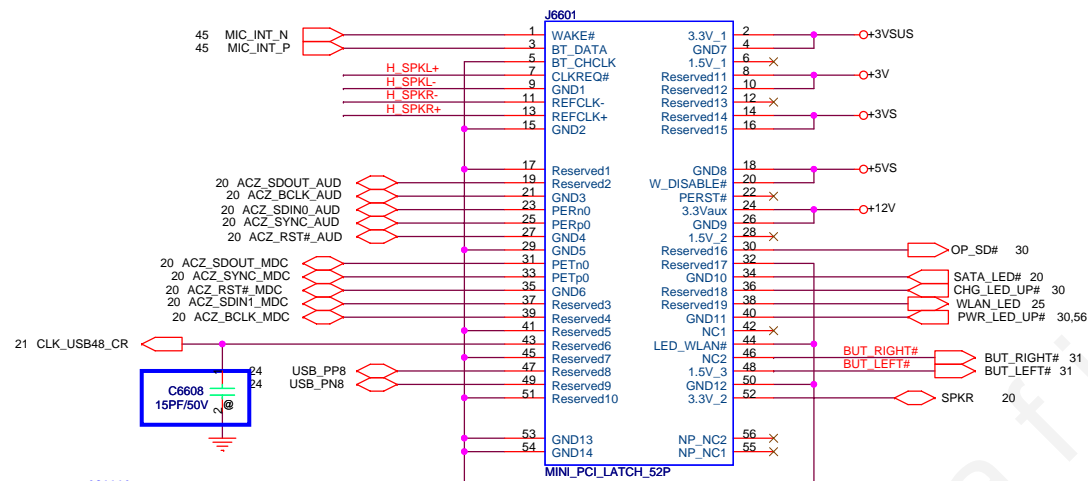


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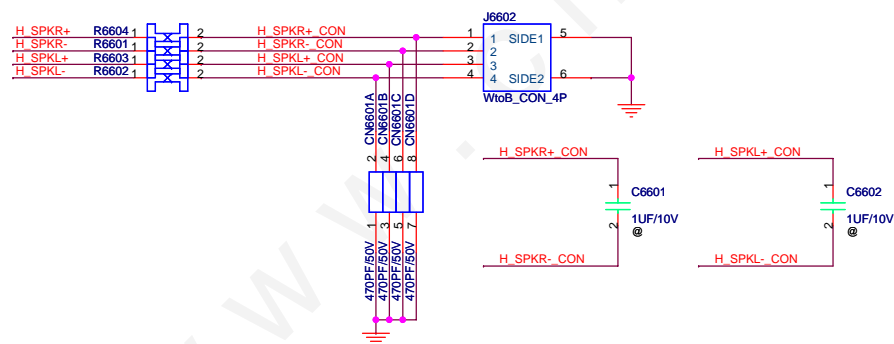
LID

SWITCH (BOTTOM SIDE)





091110
Reserved 15PF at CLK_USB48_CR For EMI Request



<<Attention>>

- If you mount the LC filter (L1-L4;C6602/C6603;CN6601A/01B/01C/01D),Please lett hem together and close to codec.
The placement of L1-L4 is the same as R6601-R6604
- If the PCB trace and Speaker wire length is less than 20cm, you don't need the LC filter(L1-L4;C6602/C6603)to eliminate the EMI,
- If L1,L2,L3,L4(8.2u) are replaced by 0 ohm/1.6A resistorator(please don't use general bead, because it may influencethe THD+N quality)
 - C6602,C6603 should be NC.
 - Please make the trace length/ Speaker wire length of SPKL+/L-/R+/R- be the same as possible as you can.
 - CN6601A/01B/01C/01D are reserved for EMI fine-tune ;

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PEGATRON		Title : HDMI_ESATA COMBO BD	
Engineer: Peter Lo			
Size A	Project Name H24Y		Rev 1.0
Date: Friday, March 12, 2010		Sheet 67 of 99	

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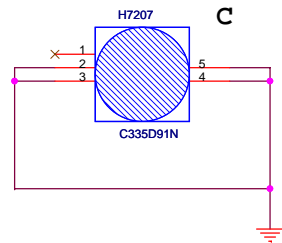
PEGATRON		Title : Small Board	
		Engineer: Peter Lo	
Size	Project Name		Rev
B	H24Y		1.0
Date: Friday, March 12, 2010		Sheet	68 of 99

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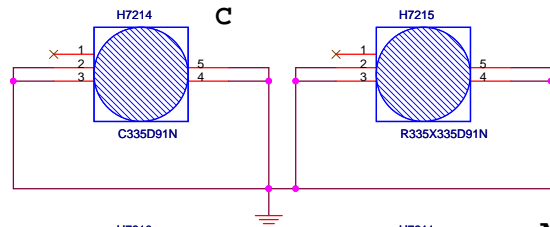
PEGATRON		Title : Audio_USB_BD	
		Engineer: Peter Lo	
Size	Project Name		Rev
B	H24Y		1.0
Date: Friday, March 12, 2010		Sheet	69 of 99

HOLES

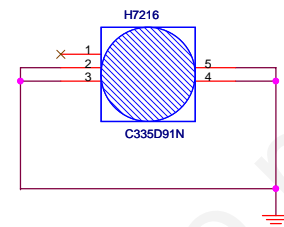
A: TOP TO BTM



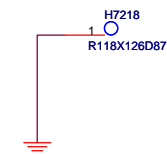
B: TOP TO BTM



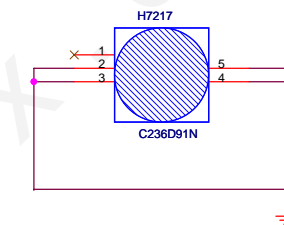
C:



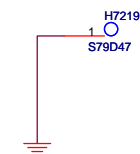
E:



D:

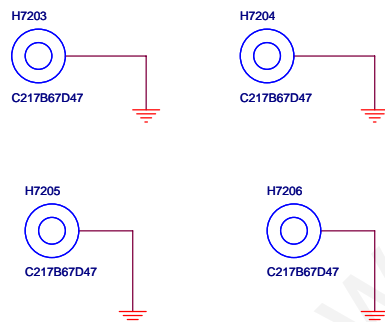


F:

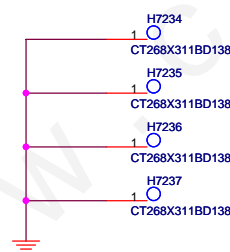


www.aitech1.ru

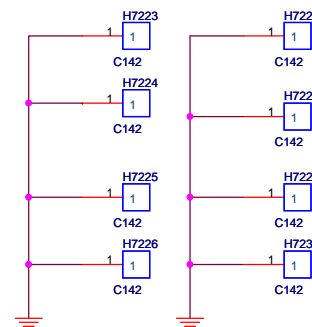
G: WLAN & FAN NUT



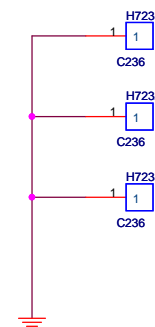
H: CPU BRACKET



I: BOSS



J: PAD



PEGATRON Title : **HOLES**

BU1-RD Div.1-HW RD Dept.3 Engineer: **Peter Lo**

Size	Project Name	Rev
Custom	H24Y	1.0
Date: Thursday, March 18, 2010	Sheet 72 of 99	

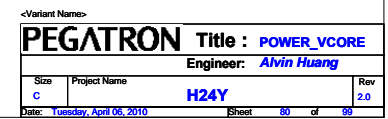
www.aitech1.ru

PEGATRON		Title : VGA(9)_****	
		Engineer: Peter Lo	
Size	Project Name		Rev
A	H24Y		1.0
Date: Friday, March 12, 2010		Sheet	78 of 99

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PEGATRON		Title : ****	
BU2/RD1		Engineer: Peter Lo	
Size Custom	Project Name H24Y		Rev 1.0
Date: Friday, March 12, 2010		Sheet 79	of 99

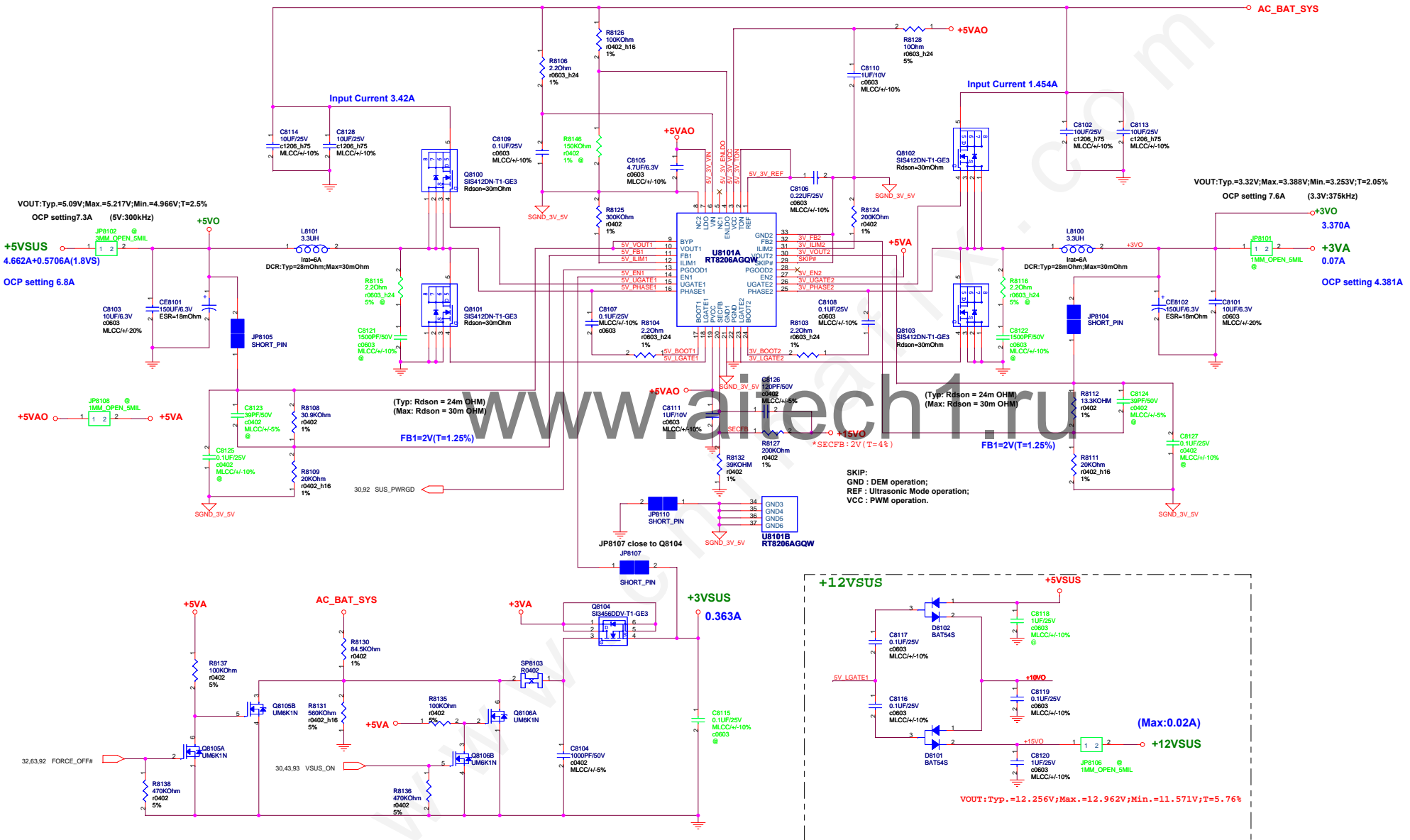
```
VID Set          DPRSLPVR='1'
VID[2:0]='111'  PSI#='0'
VID[5:3]='100'  Io=50A
VID[6]='0'
```



+5V / +3.3V POWER SUPPLY

VENLDO:
Rising Edge:Max:2V;Typ:1.6V;Min:1.2V
Falling Edge:Max:1.06V;Typ:1V;Min:0.94V

TON:(5V/3.3V)
VCC:(200kHz/250kHz)
REF:(300kHz/375kHz)
GND:(400kHz/500kHz)



<Variant Name>

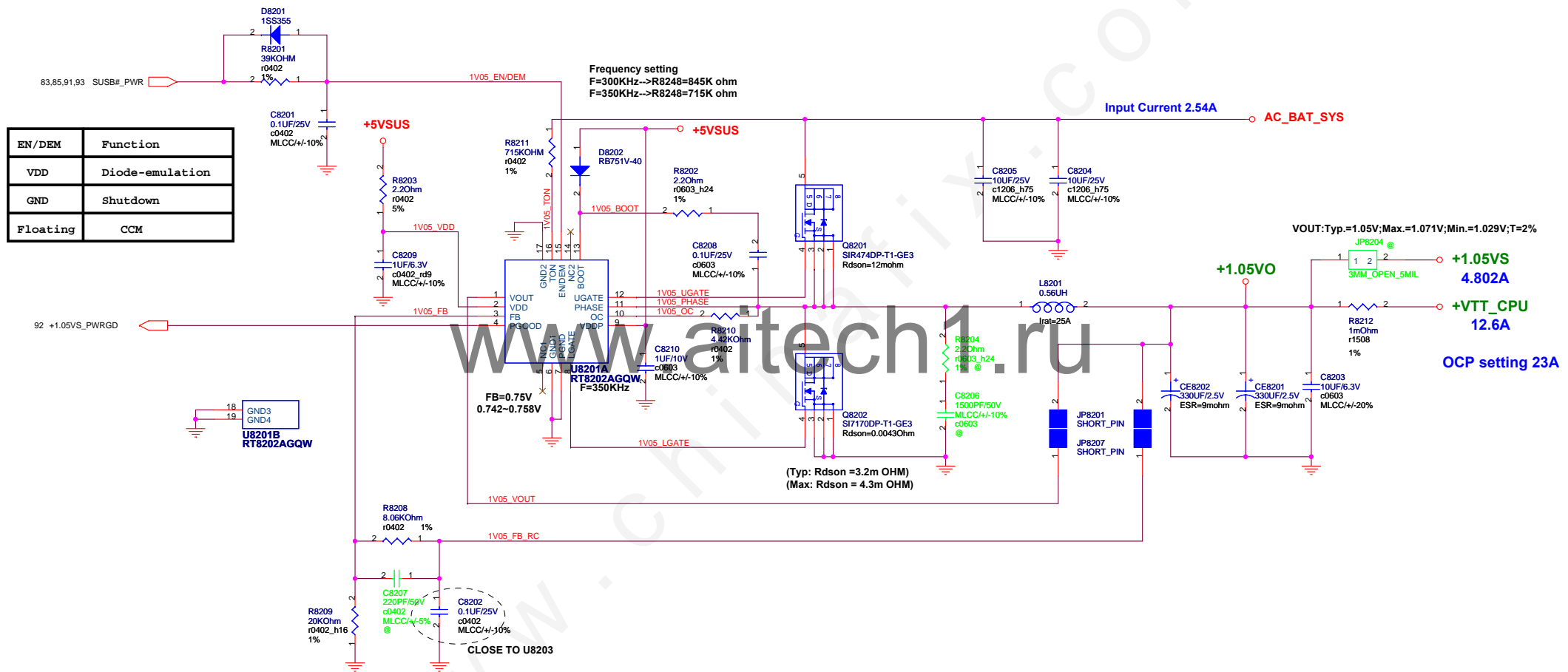
PEGATRON Title :POWER_SYSTEM

Engineer: *Alvin Huang*

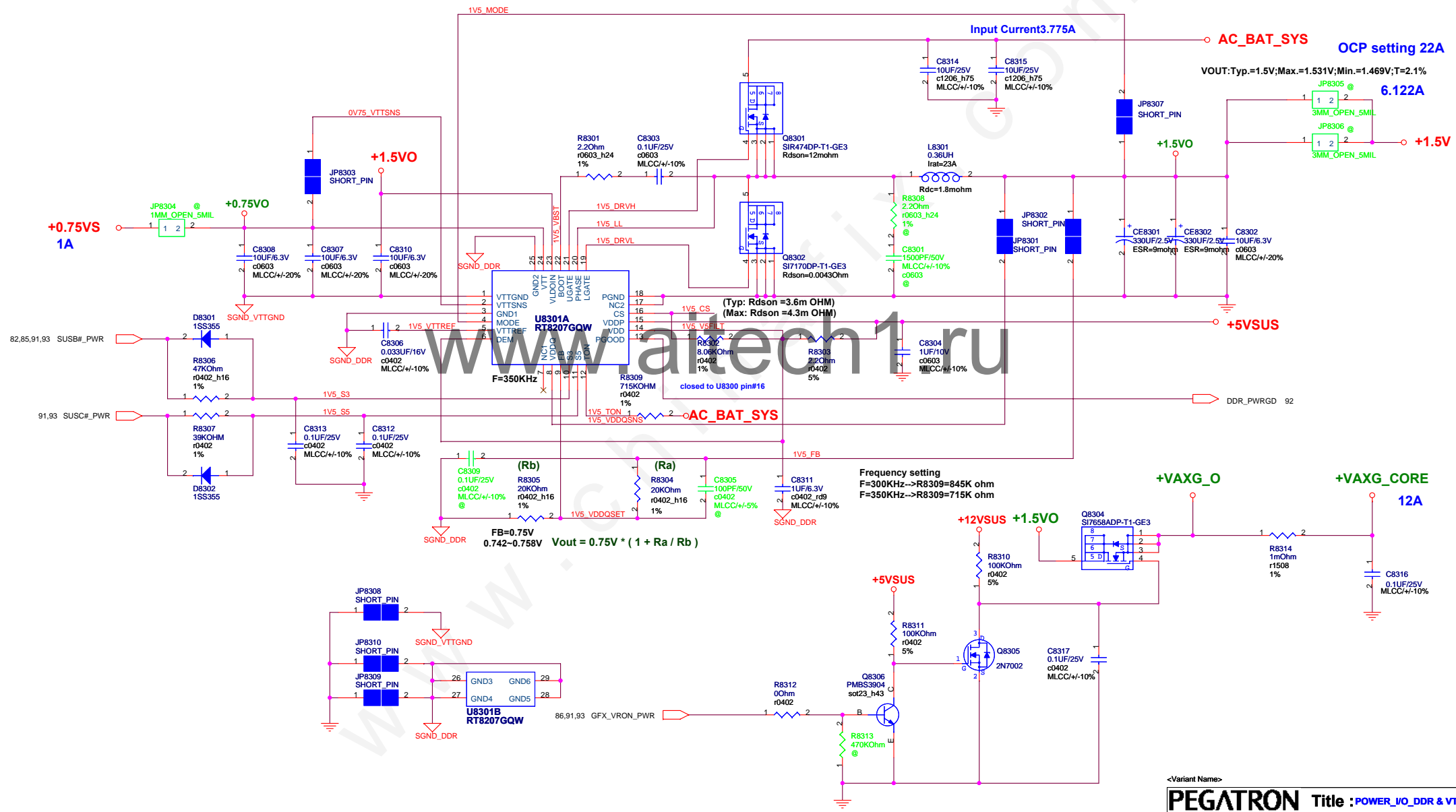
Size	Project Name	Rev
Custom	H24Y	00

Custom	H24Y	2.0
Date: Tuesday, April 06, 2010	Sheet 81 of 94	

+VTT_CPU & +1.05VS POWER SUPPLY



DDR & VTT POWER SUPPLY



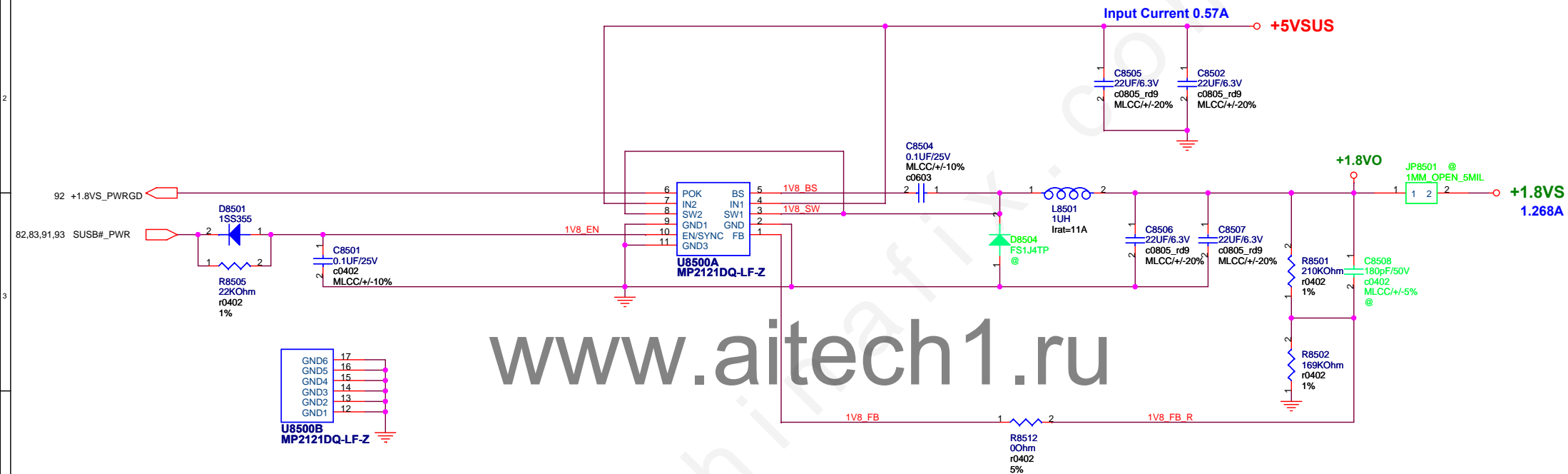
Input Current=20A*1.5V/0.8Eff/9V=4.2A

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<Variant Name>

PEGATRON		Title : POWER_N/A	
Engineer: Steven Kuo			
Size A	Project Name H24Y		Rev 2.0
Date: Friday, April 02, 2010		Sheet 84 of 99	

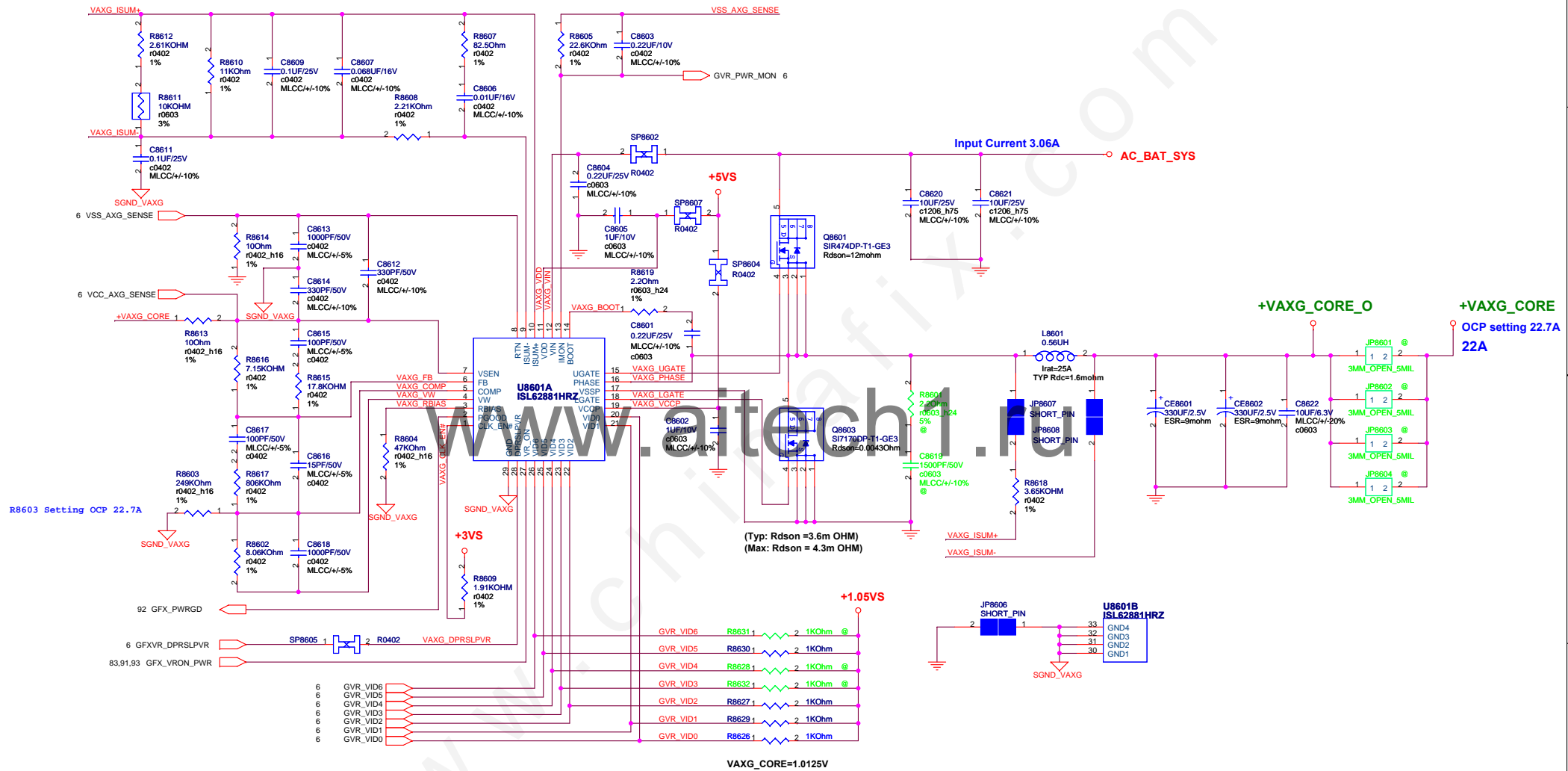
+1.8VS POWER SUPPLY



<Variant Name>

PEGATRON		Title : POWER_+1.8VS	
Engineer:		Alvin Huang	
Size B	Project Name H24Y		Rev 2.0
Date: Tuesday, April 06, 2010		Sheet 85 of 99	

+VAXG_CORE POWER SUPPLY



<Variant Name>

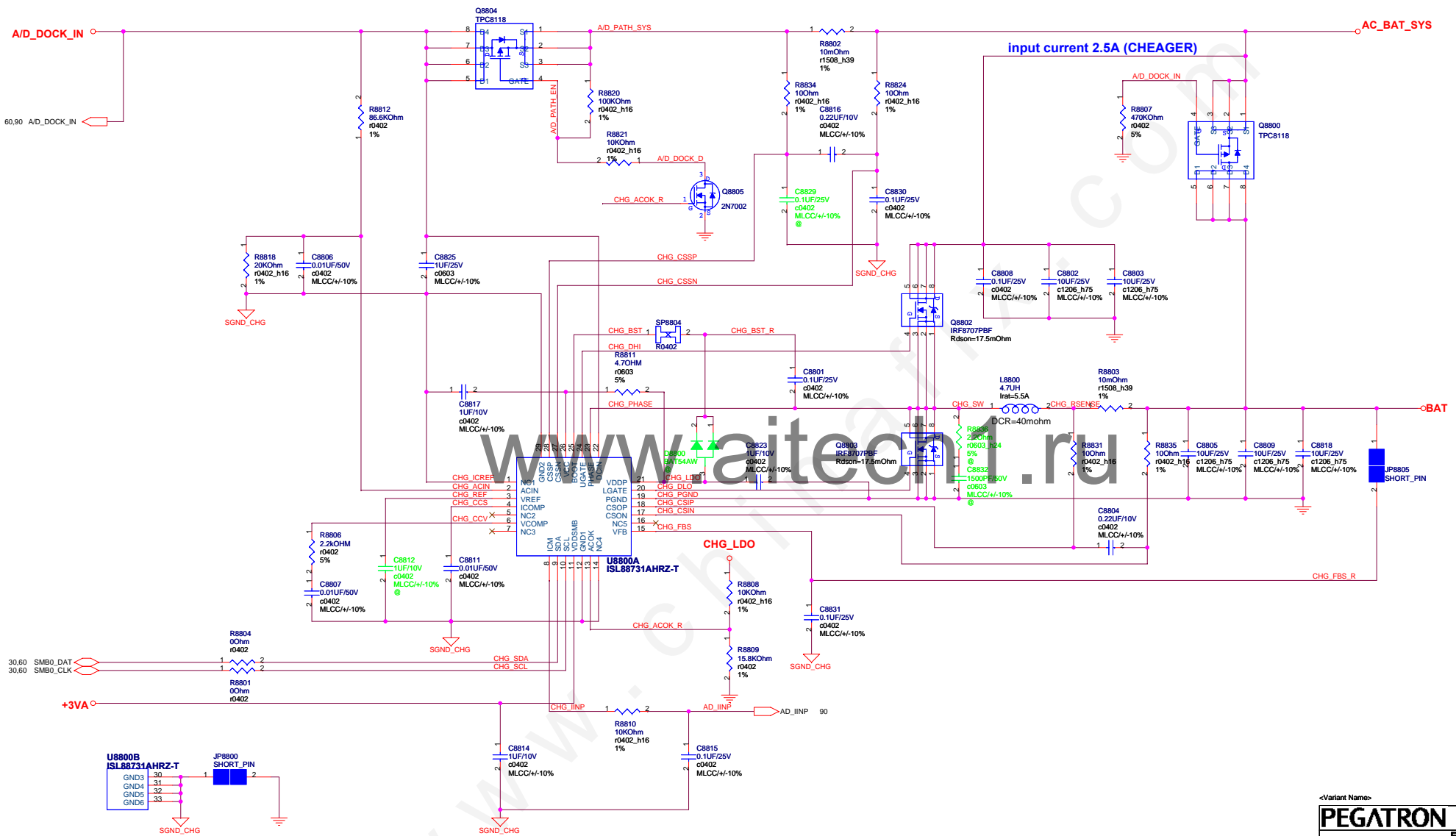
PEGATRON Title : POWER_VGFX_CORE		
Engineer: Alvin Huang		
Size	Project Name	Rev
Custom	H24Y	1.0
Date: Tuesday, April 06, 2010 Sheet 86 of 99		

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<Variant Name>

PEGATRON		Title :POWER_+VGA_VCORE	
		Engineer: Steven Kuo	
Size	Project Name		Rev
Custom	H24Y		2.0
Date: Friday, April 02, 2010		Sheet	87 of 99

BATTERY CHARGER



<Variant Name>

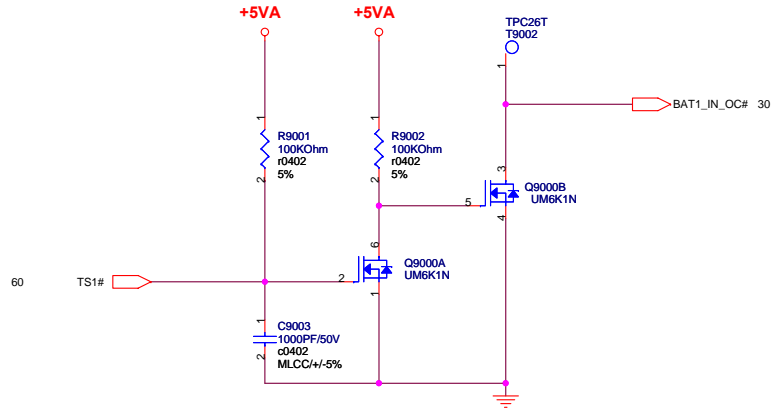
PEGATRON		Title : POWER_CHARGER	
Size		Engineer: Alvin_Huang	
Custom	Project Name	H24Y	Rev 2.0
Date: Tuesday, April 06, 2010		Sheet 88 of 99	

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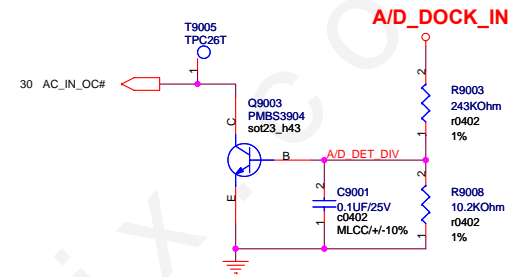
<Variant Name>

PEGATRON		Title : POWER_N/A	
Engineer: Steven Kuo			
Size A	Project Name H24Y		Rev 2.0
Date: Friday, April 02, 2010		Sheet	89 of 99

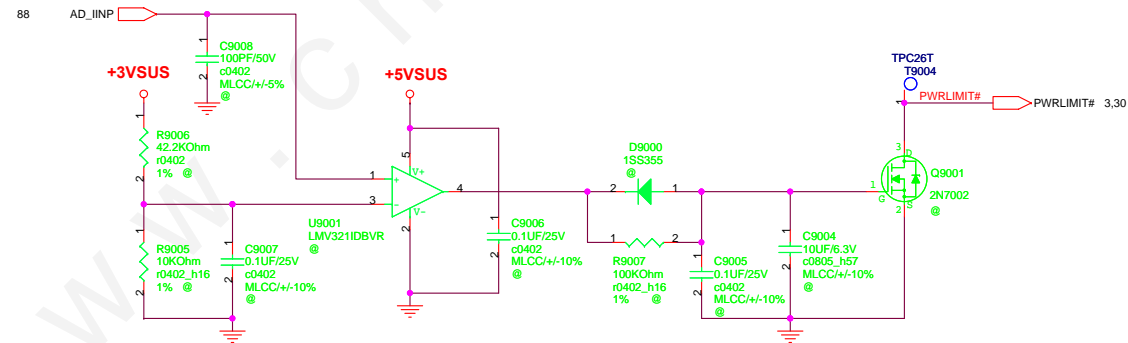
BATTERY IN DETECT



ADAPTER IN DETECT



POWER LIMIT CIRCUIT



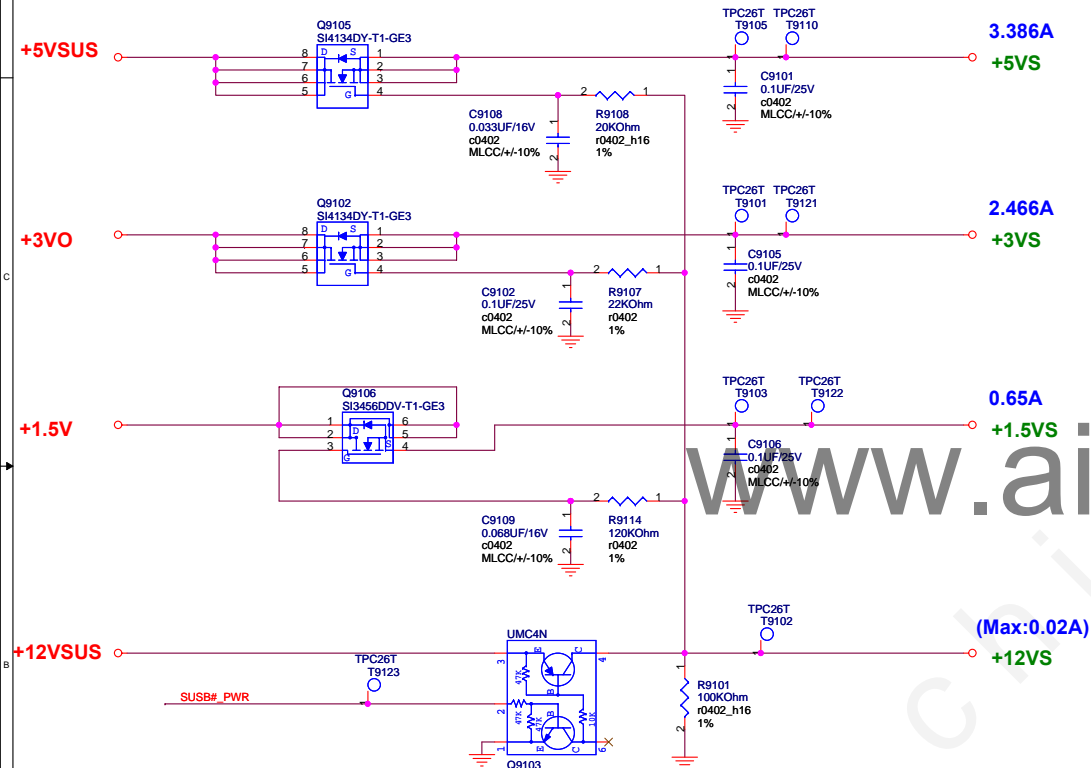
Pin_{input}=60W---->I_{input}=3.158A
R8802=10mohm
Vic_m=20*I_{input}*R8802 ==> Vic_m=0.63V

<Variant Name>

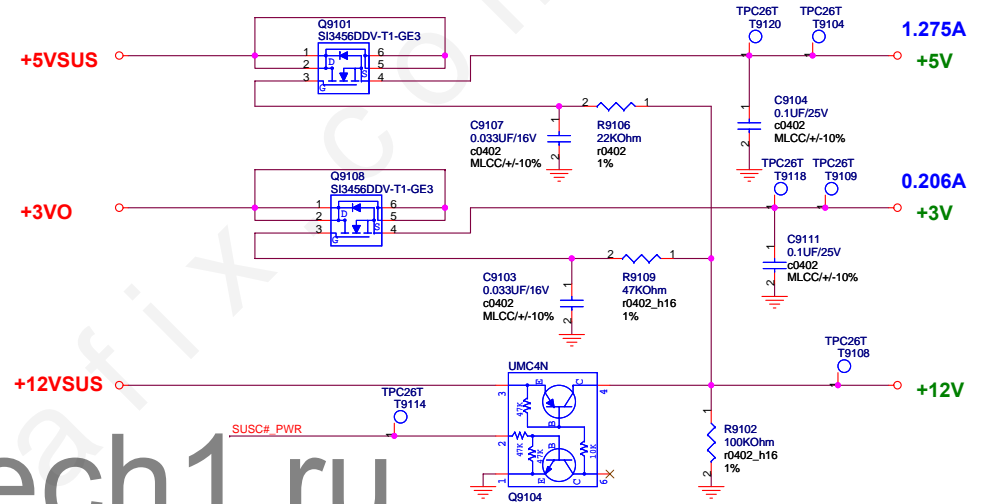
PEGATRON Title : **POWER_DETECT**
Engineer: **Alvin Huang**

Size	Project Name	Rev
Custom	H24Y	2.0
Date: Tuesday, April 06, 2010	Sheet 90 of 99	

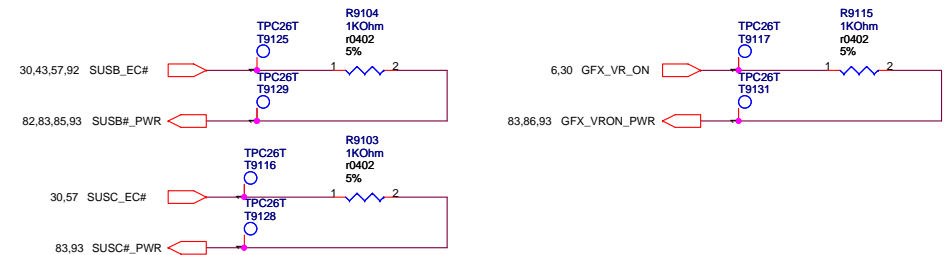
SUSB#_PWR LOAD SW



SUSC#_PWR LOAD SW



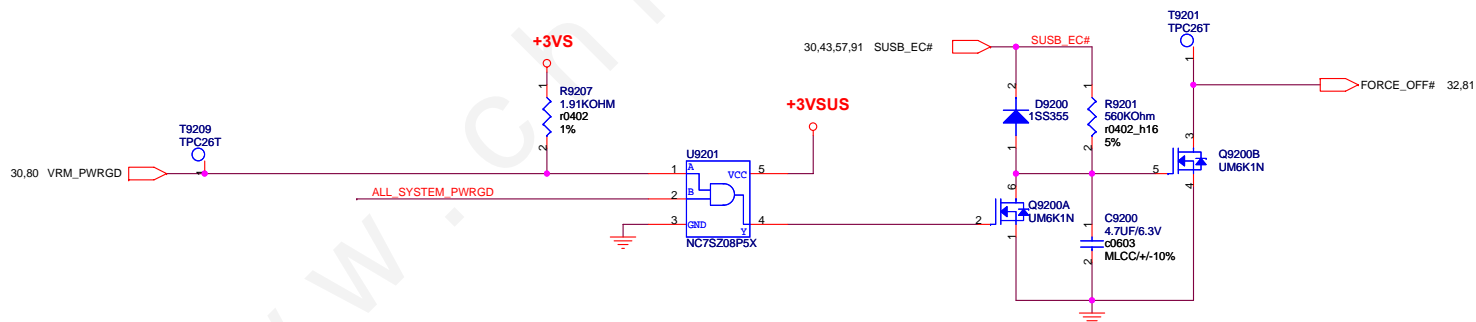
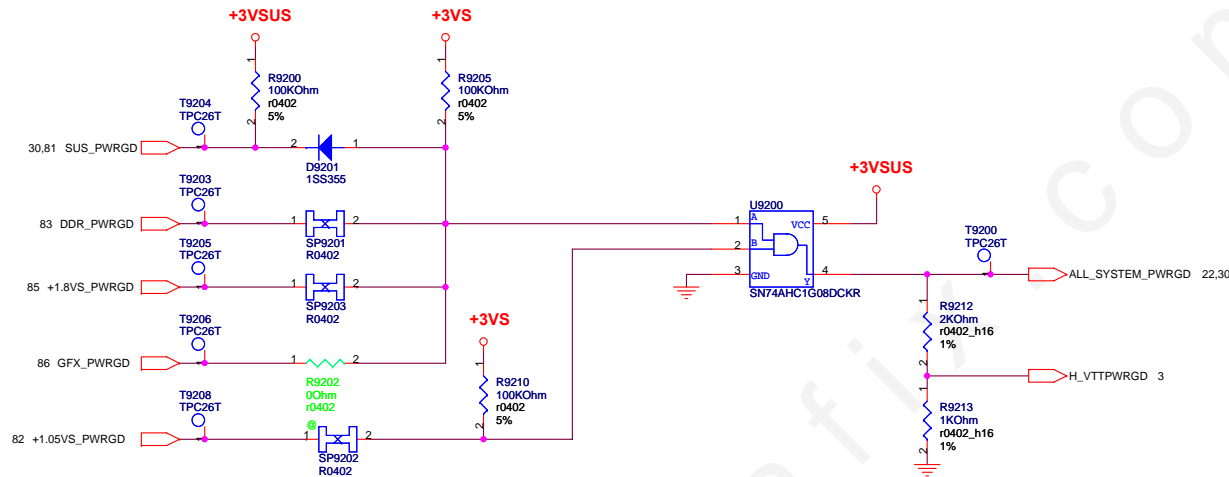
ENABLE SINGAL



<Variant Name>

PEGATRON Title :POWER_LOAD SWITCH			
Engineer: Alvin Huang			
Size	Project Name		Rev
Custom	H24Y		2.0
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POWER GOOD DETECTOR



<Variant Name>

PEGATRON Title :POWER_PROTECT
Engineer: Alvin_Huang

Size	Project Name	Rev
Custom	H24Y	2.0
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AC_BAT_SYS ○ → AC_BAT_SYS 45,47,80,81,82,83,86,88
BAT ○ → BAT 60,88

+3VA ○ → +3VA 20,30,57,63,81,88
+5VAO ○ → +5VAO 81
+5VA ○ → +5VA 81,90

+5VO ○ → +5VO 81
+3VO ○ → +3VO 81,91
+1.8VO ○ → +1.8VO 85
+0.75VO ○ → +0.75VO 83
+1.05VO ○ → +1.05VO 82

+1.5VO ○ → +1.5VO 83
+5VSUS ○ → +5VSUS 27,81,82,83,85,90,91
+3VSUS ○ → +3VSUS 21,22,24,25,27,30,33,34,43,56,66,81,90,92
+12VSUS ○ → +12VSUS 28,81,83,91

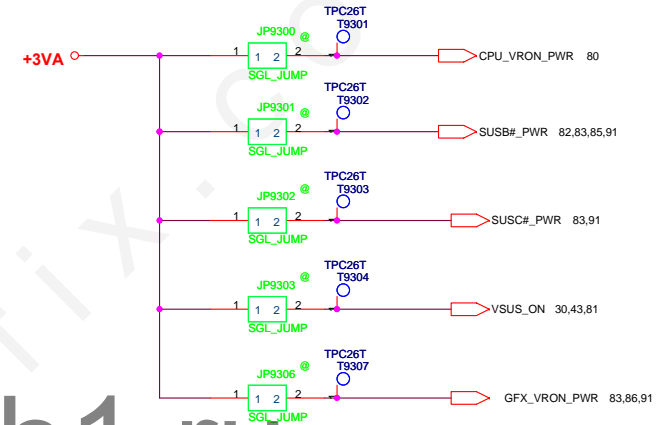
+5V ○ → +5V 45,57,91
+3V ○ → +3V 24,43,44,53,57,61,66,91
+12V ○ → +12V 52,66,91

+3VS ○ → +3VS 3,16,17,20,21,22,23,24,25,26,27,28,29,30,31,32,43,45,46,50,51,53,56,57,61,66,80,86,91,92
+5VS ○ → +5VS 27,30,31,45,46,50,51,57,66,80,86,91
+12VS ○ → +12VS 28,91
+1.05VS ○ → +1.05VS 26,27,29,57,80,82,86

+1.5VS ○ → +1.5VS 43,53,57,91
+0.75VS ○ → +0.75VS 16,17,18,57,83
+1.8VS ○ → +1.8VS 6,26,57,85

+VCORE ○ → +VCORE 6,57,80
+VAXG_CORE ○ → +VAXG_CORE 6,57,83,86

FOR POWER TEST



<Variant Name>

PEGATRON Title : **POWER_SIGNAL**
Engineer: **Alvin Huang**

Size	Project Name	Rev
Custom	H24Y	2.0
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2009/10/19

1、add jp8205、JP8206、JP8601、JP8602、Q8204、Q8203、R8620

2、Delete R8620 because have R9115 @

2009/10/20

3、Delete Q8203 for Layout

4、change R8208 to 9.53K adjust Vout to 1.1V

5、change R8043 from 2.87K to 2.7K For Loadline

6、change CE8002、CE8005 change from 470UF to 220UF and CE8001、CE8004 change from 470UF to 330UF for

7、change R8124、R8125 to 300K for OCP

8、change R8210 from 4.42K to 6.49K For OCP 30A

9、change R8616 from 7.5K to 14.7K for Loadline

2009/10/21

10、C8027 @ to N/A

11、add sp8004 and C8039

12、change R8616 from 14.7K to 6.04K,R8608 change from 4.32K to 2.1K adjust OCP(22A) and Loadline

13、P85 IC to MPS2121

2009/11/11

14、P85 add R8503,R8513;R8504;Q8502;Q8501 from N/A to @

15、L8501 2.2 to 1UH,C8506;C8507 from 10UF to 22UF

2009/11/12

16、add C8129,C8130 for EMI

17、add C8211 ;R8204,C8206 from @ to N/A

18、add C8318 ;R8308,C8301 from @ to N/A

2009/12/02

19、R8033 R8035 chane from 10K to 51K

20、R8204 R8308 chane from 0603 to 0805

21、C8206 from 1000PF to 1500PF For EMI

22、CE8201 CE8202 from 330UF to 220UF

22、R8501 to 301K, R8502 to 240K

<Variant Name>

PEGATRON			Title : POWER_I/O_DDR & VTT		
Engineer: moon					
Size A	Project Name H24Y				Rev 2.0
Date: Friday, April 02, 2010			Sheet 95 of 99		